INTEGRATED 3D GLASS MODULES WITH HIGH-Q INDUCTORS AND THERMAL DISSIPATION FOR RF FRONT-END APPLICATIONS

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INTEGRATED 3D GLASS MODULES WITH HIGH-Q INDUCTORS AND THERMAL DISSIPATION FOR RF FRONT-END APPLICATION

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SUMMARY

The objectives of this research are to model, design, fabricate and demonstrate miniaturized and high-performance RF components, thermal structures and integrated modules with advances in designs, materials and processes. High quality factor (Q > 100 at 2.4 GHz for 3-10 nH/mm^2) inductors are demonstrated with 50-100 micron thick glass using 3D designs and fabrication processes. Innovative RF design-compatible thermal structures with copper through-package vias are designed to maintain low junction temperatures of < 85 ^{o}C in power amplifier modules. Dual-band (2.4GHz/5GHz) WLAN modules are demonstrated in ultra-thin glass substrates with double-side RF circuits and copper through-package vias (TPVs).

Today's RF subsystems are 2D multichip packages that are made of either organic laminates or LTCC (low temperature co-fired ceramic) substrates. The need for form-factor reduction in RF subsystems in both z and x-y direction has led to the evolution of embedded die-package architectures in thin laminates or fan-out packages, with dies facing up or down. This also reduces insertion loss and improves signal integrity by minimizing package parasitics and routing issues. For further improvement in performance and miniaturization, Georgia Tech proposed and is developing glass as the ideal next generation substrate for RF module integration. However, major design and fabrication challenges need to be addressed to achieve ultra-thin high Q RF components and also enable RF power amplifier (PA) cooling to eliminate hotspots on glass substrates without affecting the RF performance. This forms the key focus of this thesis.

Innovative high-Q 3D inductors using through-package via (TPV)-based copper networks in ultra-thin glass substrates are developed and demonstrated in the first part of this research. Copper TPV networks that meet the PA design constraints are designed to enable heat transfer in ultra-miniaturized glass packages. Dual-band WLAN RF front-end modules with 3D or double-side thinfilm passive components on glass-based substrates and surface-assembled PA, LNA and switch are fabricated and characterized to demonstrate the benefits of glass-based RF modules.

CHAPTER 1

INTRODUCTION

Strategic Need

Wireless communications have been a key enabler for the success and prevalence of smartphones, and will play a more prominent role in automotive electronics for functions such as autonomous driving with vehicle-to-vehicle connectivity, in-car smartphone-like infotainment with vehicle-to-network connectivity, privacy and security. These applications have been driving major breakthroughs in packaging innovations for multiband communications (LTE or long-term evolution, LoRa or low-power wide-area network, WiFi, mmWave) and sensing. In order to connect one device to the other, multiple RF communication standards such as GPS (global positioning system), WLAN (Wireless local area network), GSM (global system for mobile communication) and Bluetooth coexist, and are, therefore, referred to as multi-mode multi-band (MMMB) subsystems. The current wireless systems need to be further developed to the next level, where they can simultaneously support even more frequency bands without interference between them. Further, carrier aggregation, allowing mobile network operators to combine a number of separate LTE carriers, has been a key driver for advancing hardware and software, leading to higher peak user data rates and overall capacity of their networks, and to exploit fragmented spectrum allocations.

The need for higher wireless data-rates also necessitates the use of faster communication networks. Fifth generation mobile networks, called 5G, is the next major phase of mobile telecommunications standards beyond the current 4G technology

standards. Compared to the current 4G technology, which focuses on faster peak internet connection speeds, 5G technology is expected to result in higher capacity than 4G technology, allowing much greater number of mobile broadband users per area, offering consumption of unlimited data quantities. This new technology will enable large portion of the population to access high-quality streaming media with their devices, even when Wi-Fi hotspots are out-of-reach.

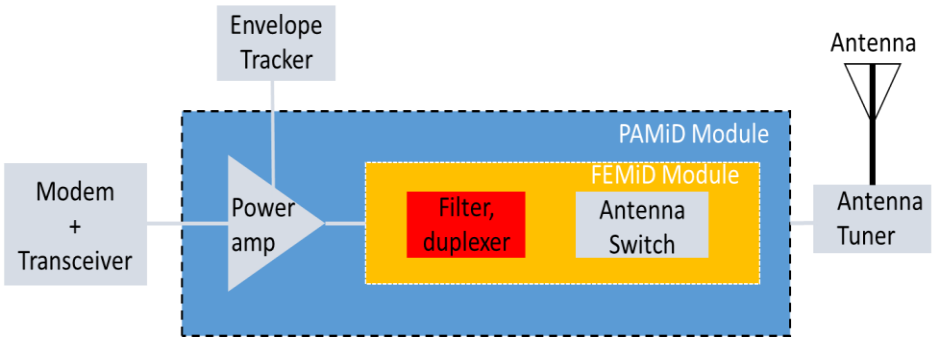


Figure 1. Block diagrams of PAMiD and FEMiD architectures in a RF Front-end module (Courtesy: Qualcomm)

This trend in communications is also enabling a new era of the Internet-of-Things (IoT), with remote wireless connectivity between any type of physical devices, vehicles, buildings, and other items. The IoT allows objects to be sensed and controlled wirelessly across existing network infrastructure, creating opportunities for more direct integration of the physical world into computer-based systems, and resulting in improved efficiency, accuracy and economic benefit. The 5G technology along with IoT (Internet of Things) concept will bring a new paradigm with improved support to machine-to-machine communications, aiming at lower cost, lower power consumption, and better performance.

Miniaturized electronic modules with increased functional density, reduced footprints and minimal interference are essential to meet the growing demand for smart mobile systems. Figure 1 shows a simple block diagram for PAMiD (power amplifier module - integrated duplexer) and FEMid (front end module - integrated duplexer) modules. FEMiD architecture isolates RF signals that are received by a mobile phone's antenna into transmission and reception signals for each communication band, and then transfers them. PAMiDs go one step further by integrating power amplifiers (PA) with the switches and duplexers, leading to a complete integration of a MMMB module on a dedicated platform. The growing demand for PAMiD and FEMiD modules are illustrated in Figure 2.

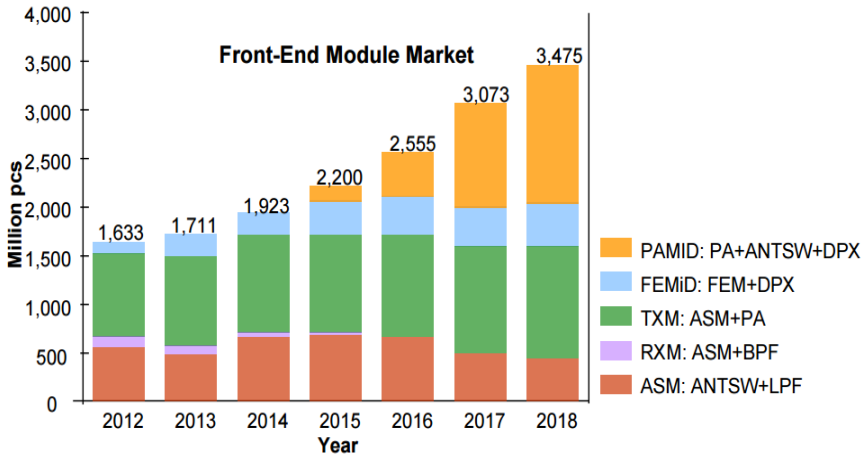


Figure 2. Recent trend in RF sub-systems for smartphone applications (Courtesy: TDK-EPCOS and Prof. Joungho Kim, KAIST).

RF Module

RF modules comprise of actives, passives and their integration into a miniaturized and cost-effective module. The variety of passive and active functions in a RF module are listed in Figure 3. This section briefly describes the recent trends in these three categories. LNAs (low noise amplifiers) and PAs (power amplifiers) are the major active components that play key roles in WLAN transceivers. As 5G era approaches, the operating frequency of interest for such key components will eventually increase up to several tens of GHz, compared to current mobile frequencies of 2.4GHz or 5GHz. Thus, the most widely used power amplifiers with CMOS technology is likely to be challenged by GaAs power amplifiers for future cell phones. They're made in a variety of frequency ranges to cover the various fixed cellular bands, with typical power level ranges from 27.5 to 28 dBm (0.4 to 0.5 W).

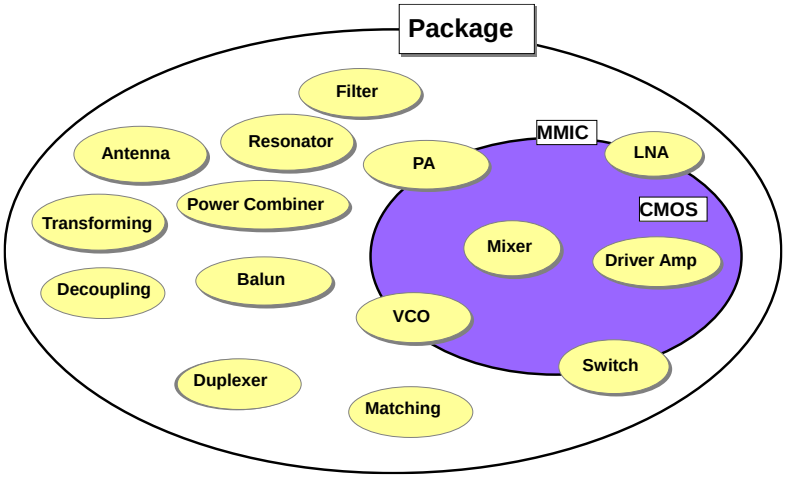


Figure 3. Active and Passive Components for RF Front-end Module
(Courtesy: Prof. M. Tentzeris)

For higher RF power levels, gallium nitride (GaN) is projected to play a dominant role because of its higher voltages levels, which are difficult or impossible to reach using

GaAs. By reducing device parasitic elements and using shorter gate lengths, and using higher operating voltages, GaN transistors have reached higher output-power densities, wider bandwidths, and improved dc-to-RF efficiencies. However, these GaN devices also require sufficient thermal management.

Passive components perform various functions, such as decoupling, biasing, resonating, filtering, matching, transforming, etc., as illustrated in Figure 3, and are therefore, an indispensable part of RF systems. Discrete and SMD solutions are, by far, the most popular approaches in the industry, and may still be dominant for some times. The trend towards passive-active integration began with enhancing the volumetric density and performance of passive components, and therefore transforming today's thick discretes to thinfilms. The passives footprint is further reduced by direct deposition of such films on separate, testable and yieldable ultra-thin glass substrates, referred to as IPDs. For certain functions (filtering, for example), IPD with thinfilms on thin glass substrates have smaller footprints and low profile (150µm - 250µm height) than LTCC counterparts, while achieving similar electrical performance. The next step towards passive-active integration is to embed the thinfilm passives in the module substrate, close to the active devices that they serve.

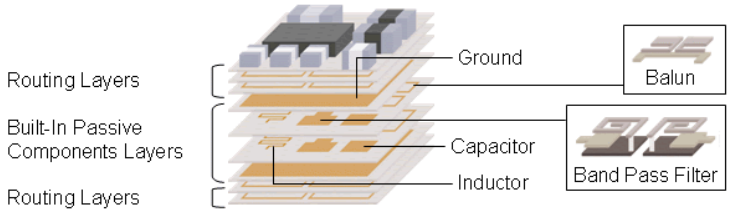


Figure 4. An example of LTCC module with embedded passive technology

(Courtesy: Kyocera)

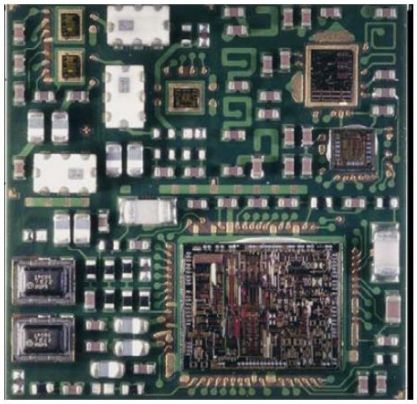


Figure 55. Laminate-based RF module (Courtesy: Skyworks)

Low substrate loss is a key metric for RF applications. LTCC and organic laminates are widely used in RF packaging. Examples of ceramic and organic RF packages are shown in Figures 4 and 5 respectively. Ceramic substrates have been well-recognized for their RF performance and module integration. The cost, flexibility and integration challenges of ceramics have led to the evolution of organic packages. Figure 5 shows a single-package radio (Skyworks, 13 mm x 13 mm Dual Band GSM/GPRS). This package integrates transceiver, power amplifiers, power management, LTCC filters, switch, SAW filters along with some SMD components on the laminate substrate. In addition, some small-value inductors are embedded inside the laminate substrate. This trend from ceramic to organic RF packaging is illustrated in Figure 6. Although, low-loss organic substrates have gained in popularity for RF applications, their poor dimensional stability and warpage, as well as their moisture-uptake pose challenges for miniaturizing RF devices and modules or subsystems.

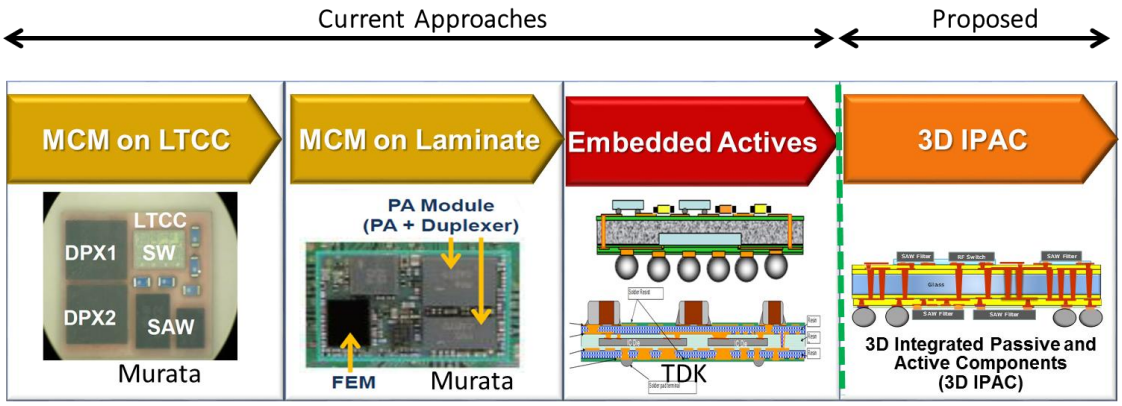


Figure 6. Evolution of RF packaging from LTCC to organic laminates, wafer- or panel-based embedding, and 3D integrated passive and actives components (3D IPAC)

The evolution of embedded wafer level fan-out technologies (eWFO) is expected to further enhance the performance, with reduced parasitics and footprint by eliminating the use of wire-bonding. Double-sided multiple re-distribution layers are formed to fan-out the transceiver input and output signals and through-mold vias are employed to realize the vertical interconnections. Panel-based embedding is emerging as another compelling alternative to wafer-level fan-out, as shown in the right side of Figure 6.

Glass-based RF packages

Glass package technology in 2D, 2.5D and 3D, pioneered by Georgia Tech since 2010, has been emerging as an ideal solution for high-performance and ultraminiaturized RF front-end modules with simultaneous reduction in both X-Y and Z directions. Glass combines the benefits of ceramic, organic and silicon. This is because glass provides many advantages such as ultra-thinness, ultra-low electrical loss, silicon-like dimensional stability, high stiffness, high Tg, high surface smoothness and adjustable coefficient of

thermal expansion (CTE). Moreover, it is superior to silicon for RF applications because it enables high-Q RF components due to high resistivity for ultra-low loss. Compared to organics, glass enables precision circuitry with finer-design ground rules because of its dimensional stability, and ability to process with ultra-thin and low-loss build-up organic or inorganic dielectrics, without process-compatibility issues. Recent advances at Georgia Tech PRC have demonstrated reliable and fine-pitch through-vias (TPVs) in glass with double-side assembly of active and passive components with ultra-short interconnections. In addition to these, glass as a packaging substrate appears to be a perfect solution for its cost effectiveness. Qualitative comparison of various substrate materials in terms of their performance characteristics, processability, reliability and cost clearly shows glass as the superior candidate, as illustrated in Figure 7.

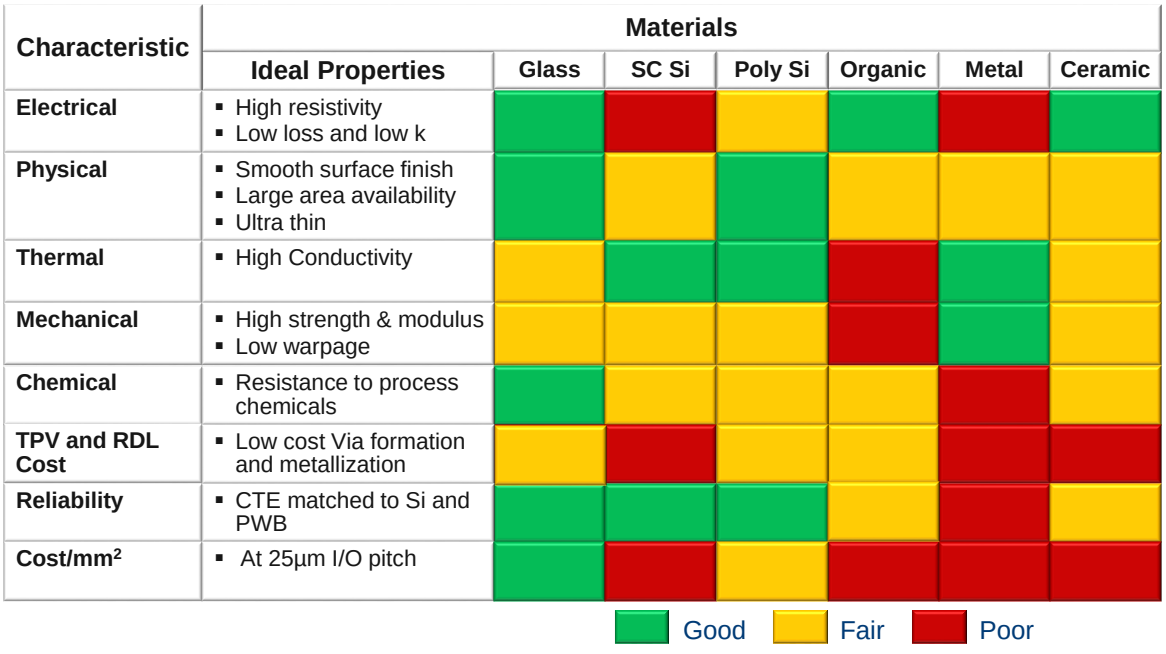


Figure 7. Comparisons of performance, processability, reliability and cost of various types of substrate materials (Courtesy: Prof. Rao Tummala)

TPVs enable double-side integration of components, thus reducing the X-Y footprint of the modules by about half. Further, the ability to surface-mount active and passive devices with high precision reduces the interconnect length between actives and passives. Glass is as also an ideal material for realizing passives because it combines the benefits of ceramics for ultra-low loss, and organic packages for large-area and low-cost processing, and silicon for high-density and lithographic precision. Formation of polymer or inorganic build-up dielectrics with low loss (loss tangent < 0.005) and high dielectric constant onto these thin glass substrates enable high capacitance and inductance densities with high Q-factor. Fine-pitch through-via formation using low-cost substrate processing tools and processes such as laser vias and double-side wet metallization techniques allows interconnecting the components on both sides with standard panel-processes at lower cost.

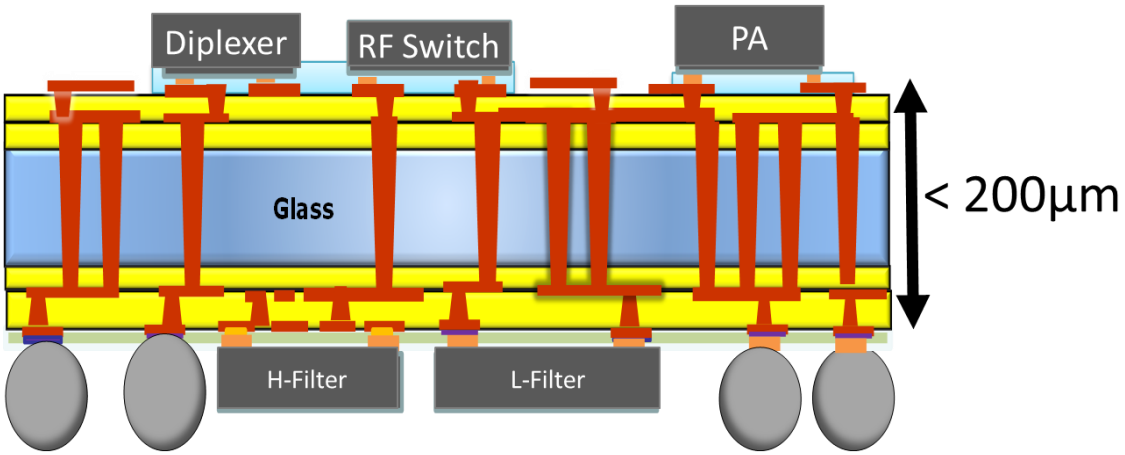


Figure 8. Conceptual cross-section of 3D IPAC RF modules with glass
(Courtesy: Dr. Junki Min and Zihan Wu)

Research Objectives, Challenges, and Tasks

Research Objectives

The objectives of this research are to model, design, fabricate and validate high quality factor (Q > 100 at 2.4GHz for 3-10nH/mm^2) inductors with innovative 3D structures in ultra-thin glass. Innovative RF design-compatible thermal structures with copper through-package vias are designed to maintain low junction temperatures in power amplifiers, while also meeting PA compatible design rules. Demonstration of ultra-thin Dual Band (2.4GHz/5GHz) WLAN modules or subsystems with passive-active integration on ultra-thin glass substrates with double-side RF circuits and copper through-package vias (TPVs) forms the final objective of this thesis. The detailed objectives, prior art and challenges are summarized in Table 1 and described in subsequent sections. A schematic cross-section of the proposed module is shown Figure 9.

Table 1. Objectives, Prior art, Challenges and Research Tasks

Labels	Targets	Prior Art	Challenges
A. High-Q inductors	• 3-5nH for 1 mm^2 • Q>100 @ 2.4GHz • Thickness: 50-100 microns	• Q: 50-60 at 2.4 GHz • 250-600 microns • 2D or 3D Inductors in organic laminates; • 3D inductors in thick glass;	• Low inductance from low magnetic flux coupling in thin glass • Losses from capacitive coupling and skin-effect
B. Integrated cooling with Cu TPVs in glass packages	• Steady-state Temp. at Hotspot < 85°C	• Bulky heat sinks and heat spreaders	• Integrated Cu thermal structures without affecting PA performance

Table 1 continued

C. Dual band WLAN module	• LNA, PA and switch in ultraminiaturized module; • Loss from entrance to exist port: 0.5-1 dB; • Substrate thickness: 200 microns (3X reduction)	• Loss of >2 dB • 0.6 mm thickness	• Precision RDL and through-vias with ultra-thin glass

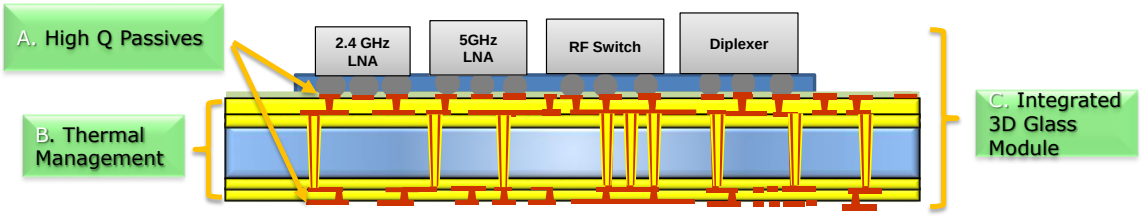


Figure 9. Proposed dual-band WLAN module on a glass substrate.

Research Challenges and Tasks

Major fundamental challenges are foreseen in achieving the program objectives. These challenges and the research tasks to address them are described in this section.

Research Challenges - High-Q Inductors

Passive-active integration requires two advances: miniaturization of thick inductors as thinfilms while retaining their high Q factor, and integrating them into the package substrate with ultra-short distance to other passive networks and active devices. However, this leads to Q factor degradation because of several factors such as substrate losses, high ratio of resistance to inductive reactance because of skin effect, proximity and parasitic capacitance between tightly-spaced conductors. Thus, it is inevitable to place the inductor off the chip, in the package, to overcome the constraints from limited

on-chip real-estate and high losses. Moreover, it is beneficial for the components to utilize the substrate volume in all three (X-Y and Z) directions. Therefore, size-performance trade-off in the components can be enhanced with more flexibility in the design options.

Traditional spiral inductors have achieved high inductance density by winding copper traces as 2D coplanar or 3D multilayer coil structures, while achieving relatively high Q factor (~40) by designing with the proper ratio of line width and spacing. Despite the ease in controlling the inductance density and achieving adequate Q factors for certain RF applications, 2D inductors still face trade-offs in simultaneously achieving high Q and inductance density. In order to achieve higher Q factor, more induced magnetic flux is required while keeping the resistance as low as possible. Moreover, trade-offs between inductor size, Q-factor and inductance density should be thoroughly balanced to meet the targets for RF matching networks in the required foot-print. Process variation in line-width and spacing can deviate electrical performance. Lastly, process challenges with low-loss dielectrics on ultra-thin glass creates additional challenges for high-Q.

Research Tasks - High-Q Inductor

a. Modeling and design: This subtask focuses on modeling and design of innovative 3D inductors with suppressed proximity effect and parasitic capacitance in order to achieve high quality factor, while satisfying all other specifications. Spiral 2D inductors will be compared with 3D TPV inductor options in thin glass, in terms of density and Q. The

impact of stacked high-permeability nanomagnetic films on enhancing the inductance of 3D inductors will be studied through modeling and design.

b. Fabrication and Characterization: This subtask focuses on fabrication and characterization of innovative 3D inductors in order to correlate the simulation results with the actual measurement data. Trade-offs associated with glass thickness will be investigated through design, fabrication and characterization. The validated models will be utilized for subsequent design optimization. The specific objectives of this task are listed in Table 2.

Table 2. High Q inductors: Objectives, prior art, challenges and research tasks.

Parameter	Objectives	Prior Art	Challenges	Research Tasks
Performance with miniaturization • nH /mm^2 •Q at 2.4GHz •SRF •Glass thickness (μm)	• 3-5 • 100 • > 10GHz • 50-100	• 3-5 • 50-60 • 8 GHz • 200-600	• Trade-offs in Q and inductance density • Losses from dielectric, conductors, flux leakage, capacitive coupling and ground proximity • Limited Q enhancement with 2D spiral inductors; • 3D inductors with solenoid structures utilize thick TPVs	• Modeling and design optimization of 3D inductors
			• Introduction of magnetic films enhances inductance density but creates additional losses	• Model and design with nanomagnetic films

Table 2 continued

Precision	• `	• 10-15% with organic laminates	• Process challenges with low-loss dielectrics on ultra-thin glass • Nonuniform plating across large panels	• Process Development with 50 micron glass • Analyze the deviation in inductance characteristics with different line space/width and TPV Cu geometries • Inductor fabrication and characterization.

Research Challenges - Thermal management with Cu TPVs

Glass is an excellent RF material, especially for its low loss, surface smoothness and dimensional stability for precision impedance matching, but the disadvantage comes from its low thermal conductivity. Thus, it is critical to embed highly-efficient thermal structures when glass packages are designed. Incorporation of copper thermal structures can degrade the electrical performance due to their coupling with the PA on-chip circuits and adjacent copper networks that are utilized for the electrical signal paths. Therefore, it is also critical that the copper thermal networks do not degrade the electrical performance. The thick Cu structures in glass should also meet fabrication constraints and reliability targets.

Research Tasks - Thermal management with Cu TPVs

Innovative Cu TPV structures are designed to cool the power amplifier (PA) dies with minimum package footprint. The Cu network design should provide adequate conduction path but minimize electrical coupling with the PA circuitry and not affect its performance. The Cu TPV network should be also optimized so as to not interfere with the TPV signal paths.

a. Modeling and design of Thermal through-vias on glass substrate: TPV copper networks that meet various electrical, fabrication and reliability design constraints are proposed to cool the hotspot of the die. The thermal performance of copper vias will be simulated through different parametric scenarios with various PA die options, hotspot options, TPV design options, and blind via options.

b. Design of thermal structures that are compatible with PA design and performance:

Glass packages with Cu TPV thermal structures are proposed to be fabricated, followed by the thermal chip-assembly, and characterization of the thermal performance with two different methods - thermal diodes in the chip and IR scope – in order to capture the temperature of a localized area on the PA chip during heat dissipation. The validated thermal models will be used for subsequent design optimization of Cu TPV network for PA cooling.

The specific objectives, prior art, challenges are research tasks are compiled in Table 3.

Table 3. Integrated cooling with Cu TPVs:

Objectives, prior art, challenges and research tasks

Objectives	Targets	Prior Art	Challenges	Research Tasks
•Integrated cooling with Cu TPVs in glass packages	•Steady-state Junction temp. of < 85°C	•PA die cooling with bulky Cu structures, heat-sinks and heat-spreaders	•Integrated Cu thermal structures without affecting PA performance •Cu TPVs should also meet reliability and fabrication constraints	•PA module design with integrated Cu TPV: parametric analysis; •Thermal PCB designs for corresponding PA modules •PA module fabrication, characterization and model validation

Research Challenges - Integrated 3D Glass Module (WLAN Module)

Fully-integrated WLAN modules with both transmitter and receiver functions requires several advances in module design. Precision RF circuits with impedance-matched low-loss transmission lines for low insertion loss from entrance to exit ports becomes critical. Electromagnetic interference (EMI) isolation between PA and LNA, and other RF components also becomes a challenge, which requires compartmental shielding or shielding at component level. Thermal issues need to be addressed because the high-power densities in PA create hotspots. Glass is an ideal substrate for RF module integration. However, several fabrication advances are required to realize 3D IPAC modules in Figure 8. These include fabrication of precision RF circuits on either side of glass, through-package vias in glass and surface-assembly of actives with high component density, which requires low warpage.

Research Tasks - Integrated 3D Glass Module (WLAN Module)

Fully-integrated dual band (2.4GHz and 5GHz) WLAN Rx modules with low-noise amplifier and RF switch are proposed to be fabricated with ultra-thin 3D glass packages. The sub-tasks are: 1) RF module design and layout, 2) Fabrication of 3D glass module with fine-line and double-side RF circuits and Through-package-vias, and 3) Assembly of actives onto glass package. The specific objectives, prior art, challenges are research tasks are compiled in Table 4.

Table 4. Dual-band WLAN module: Objectives, prior art, challenges and research tasks

Labels	Objectives	Prior Art	Challenges	Research Tasks
•Dual band WLAN module	•LNA, PA and Switch in an ultraminiaturized module; •Loss from entrance to exit port: 0.5-1dB; •Substrate thickness: 200 microns (3X reduction)	•Individual PA, LNA and switch packages mounted on 2D packages •Loss of >2 dB, •600 micron thickness with LTCC and organic laminates	•Precision RDL and through-vias with ultra-thin glass •EMI and thermal challenges	•Module design of ultrathin 3D IPAC glass package with double-side circuitry and through-package vias; •3D IPAC substrate fabrication •Surface-assembled actives; •Module-level characterization;

The key elements of the proposed 3D IPAC module are double-side thinfilm RF circuits with TPVs, active and passive component assembly onto the package, along with LGA connections to the board. An innovative double-via process, starting from prefabricated vias in bare glass, polymer filling and via opening, is utilized for a robust and high-yield fabrication process. Standard package panel processes are utilized for low-cost scalability to high volume manufacturing. This is followed by single-side assembly

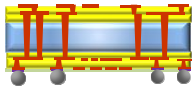
and reflow of commercial diplexer, RF switch, and 2.4GHz/5GHz LNAs. The fabricated ultra-thin (200 μm) glass substrate with 100 μm glass core, fine-pitch TPVs, fine-line RDLs and assembled actives and passives are then assembled onto the PCB with printed solders and reflow. The performance (RF Gain and Noise Figure) of completely-assembled RF WLAN module is characterized with high-precision RF GSG probes. The performance benefits of Rx part of WLAN system (2.4GHz and 5GHz LNA) with 3D glass packages will be benchmarked with state-of-the-art LTCC and organic laminate packages.

CHAPTER 2

LITERATURE SURVEY

RF Passives components provide functions such as filters, matching networks, resonators and Electromagnetic interference (EMI) isolation [1][2]. The performance metrics depend on the application. For example, the key metrics for RF filters are insertion loss in the pass-band and out-of-band rejection. Higher component performance, proximity to active devices for superior system performance and size reduction have been the primary drivers for passive component evolution. These drivers have resulted in a continuous reduction in passive component thickness from 0.5 mm in the past, to 0.15-0.3 mm, with case size of 1×0.5 mm^2 or 0.5×0.25 mm^2, resulting in module thicknesses of ~1 mm. This trend in passive components is shown in Figure 10.





RF Component	LTCC	SAW/BAW	IPDs	3D Glass IPDs
Component density				
Performance				
Thickness				
Size				
Manufacturing Readiness				

Figure 10. Examples of Integrated Passive Devices (IPDs): left: diplexer with LTCC-integrated capacitors and inductors, middle: packaged SAW filters, right: glass-integrated LC networks.

Reduced passive footprint increases the component density but at the expense of placement costs. Passive arrays and IPDs (Integrated Passive Devices) have evolved as an alternative approach to reduce the component count, placement cost, footprint and interconnection parasitics. Glass-based 3D IPD structures are schematically illustrated in Figure 11.

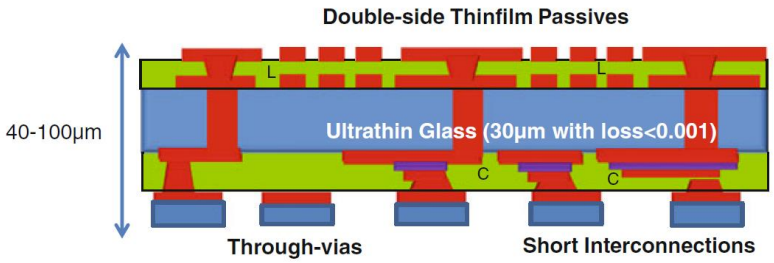


Figure 11. Schematic cross-section of glass-based 3D IPDs.

Today's passive component technologies, shown in Figure 12, face fundamental challenges in achieving adequate densities and efficiency with the required form-factors. The challenges arise from inferior materials properties with current microscale materials, process compatibility issues and the need for low-cost deposition of structures and geometries with the required properties. Advanced in high Q inductors will be reviewed in the first part of the chapter.

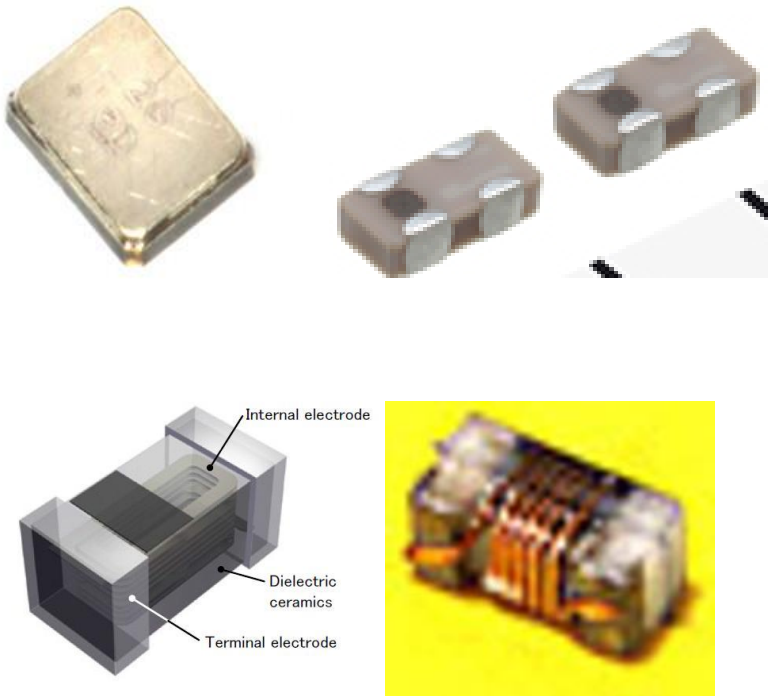


Figure 12. Today's discrete passive components (Courtesy: EPCOS, Coilcraft)

RF modules include other system-level concerns beyond the performance of individual passive components. Traditional passive components are individually packaged and mounted far from the active ICs. They add parasitics, which scale with interconnection length and deteriorate the module performance [3][4]. These include interconnect losses from transmission lines, vias and off-chip interconnections, thermal management of power amplifiers, electromagnetic interference (EMI) between various actives and passives, and other reliability challenges. Low-loss substrates with precise transmission lines for impedance match and low signal losses form the starting point for RF module integration. Other innovations related to incorporation of thermal structures, and advancing the substrates to thinner geometries and 3D embedded or doubleside integration will be reviewed in the second half of this chapter.

High-Q inductors on package substrates

The trend to carrier frequency aggregation with closely-separated carrier frequencies in the same band, imposes stringent requirements on filter rejection characteristics, cross-isolation between the aggregated frequencies, and loss budget in the RF front-end module. These translate to inductors with high density (10 nH/mm^2), high Quality factor (Q ~100), precision (2% tolerance) and low insertion losses. While on-chip inductors can easily achieve the density and precision, the high substrate losses degrade the overall performance. Innovative concepts based on trap-rich high-resistivity silicon substrates or porous silicon substrates are emerging to address this barrier. However, embedding off-chip thin-film inductors in the package substrate is a more widely-accepted solution.

In order to reach the performance metrics, a variety of inductor topologies have been explored on various package substrates such as organic laminates and glass. Two commonly-used topologies are spiral and helical inductors.

Spiral inductors: Spiral inductors typically comprise of planar coils that are embedded in the substrate core or build-up layers [14] as illustrated in Figure 13. The magnetic flux is orthogonal to the plane of the substrate. The inductance can be increased by increasing the number of turns, reducing the spacing between turns and also by employing multilayered spirals, where there is an inductive coupling between the spirals on adjacent layers that are one above the other. However, not all these techniques can yield very high quality factor. The Q reduces with increasing coil resistance. Further, the conductivity of the substrate material, on which the inductors are realized, plays a vital role in

determining the Q [15][16]. For a given inductor design, the Q will be higher if the substrate resistivity is higher.

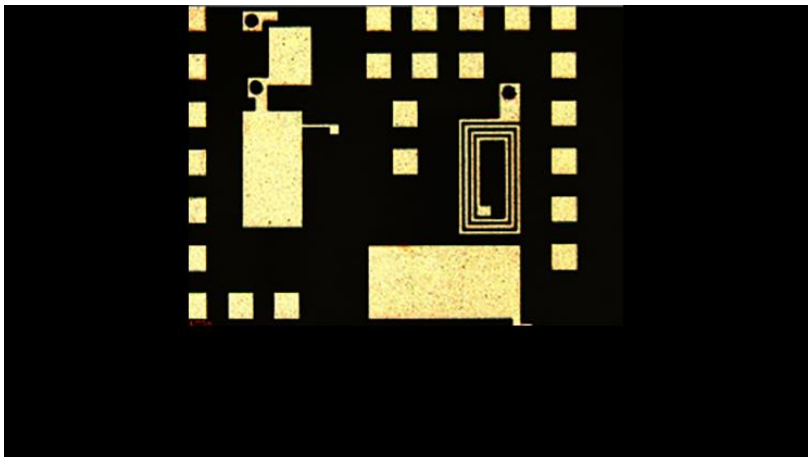


Figure 13. An example of substrate-embedded spiral inductor (Courtesy: Zihan Wu)

The design strategies for high-Q spiral inductors involve: a) larger metal thickness leading to lower resistance, b) wider traces having lower resistance, c) large central opening area resulting in higher magnetic flux, d) isolated or patterned ground planes and other metallic structures, e) incorporating shields structures [17], and f) using magnetic materials with high permeability [18]. In combination with low-loss polymer build-up dielectrics (dielectric loss of ~0.002), and organic laminate core substrates, multilayered inductor structures can be built without significant degradation in Q. With this strategy, RF inductor design libraries for density of 10-20 nH/mm^2, Q of above 70-100 and self-resonant frequency (SRF) of above 10 GHz were built with various substrate geometries and design rules [19]. With on-chip inductors, on the other hand, the metal thickness is limited to a few microns, while silicon substrates have low resistivity. Therefore, the maximum Q for on-chip inductors is limited to 10-20 [20]. Extensive research has been

reported on high Q inductors in both LTCC, organic and glass substrates. Chickamenahalli et al. [21] designed, fabricated, and characterized embedded RF inductors on organic substrates, which can substitute costly on-chip inductors. Compared to on-chip inductor, the substrate embedded inductor allow the removal of the first-level interconnect bumps beneath them to maintain a reasonably high Q value. Not only the substrate embedded inductor promises higher quality factor (Q) and lower cost than on-chip inductors due to larger available real-estate, it also allows to eliminate the need for bump array depopulation and, thus, minimizes the potential reliability issue caused by voids in the epoxy underfill between the die and the substrate.

Another innovative approach is inkjet-printed high-Q RF inductors on paper with ferromagnetic nanomaterial as illustrated in Figure 14. In this paper [22], for the first time, meander type inductors were demonstrated utilizing inkjet-printing technology on organic paper substrates. It is reported that quality factor of up to 25, inductance values of up to 8nH, and SRF of 8 GHz were achieved using this unique technology. Besides inkjet-printed inductors, magnetic materials were integrated into package so that the performance of RF and power inductors can be further improved [23].

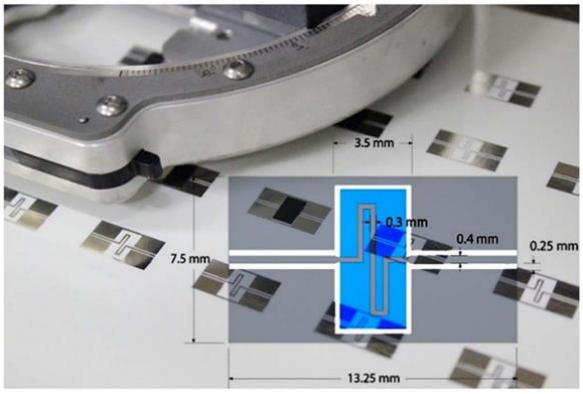


Figure 14. Inkjet Printed High-Q RF inductors on Paper Substrate With Ferromagnetic Nanomaterial. [22]

Glass is a much superior material for high inductance density and Q because it combines the benefits of: a) ceramics for ultra-low loss, b) organics for large-area and low-cost processing, and c) silicon for high-density and precise coil definition. Planar spiral inductors designed with sufficient distance from the ground planes resulted in an inductance density of 10 nH/mm^2 and Q of 30-40 on glass substrates, but 10X thinner than organic laminate-embedded inductors. Higher inductance density, without compromising Q from the resistance and capacitive parasitics, however, remains to be addressed.

Helical inductors with through-vias*:* With 2D inductor topologies, the limitation of the substrate area in X-Y direction creates trade-offs between area and high Q. Thus, in order to achieve higher Q factor, topologies with 3D inductors were investigated with innovations in design and process. The main elements of 3D inductors [24-26] with high Q factor are thick copper traces and several numbers of through-package-vias as illustrated in Figure 15, which play key roles in determining the electrical performance of the inductors. Especially, properly-designed through-vias are the most essential part to reduce the conductor resistance, which, in turn, improves Q factor. In this regard, Joyce H. Wu et al [27] thoroughly investigated the impact of through-substrate copper-damascene interconnect technology in silicon with minimal impedance. The author developed a versatile through-substrate interconnect technology with minimal impedance which allows for backside routing of power, ground, and signals for 3D and SiP

integration, low-ground inductance for RFICs, substrate noise isolation for mixed-signal circuits, and a backside contact for MEMs. The fabricated via arrays with diversified aspect ratios were characterized with the inductance, resistance and sidewall capacitance of vias. The measured S parameter of the through-substrate vias show that the copper via can be represented by a simple equivalent circuit of a resistor and inductor in series. These characterized data in the through-substrate vias provides the basis for vias to be integrated into passive circuitries and 3D inductors.

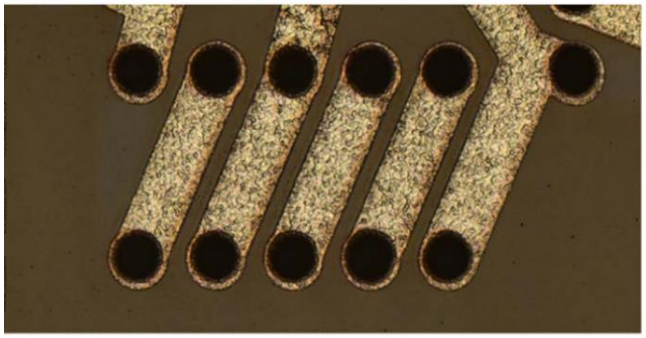
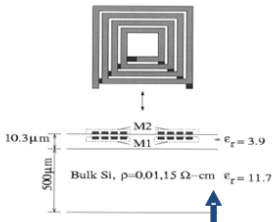
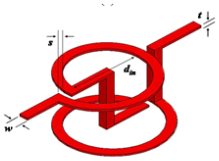


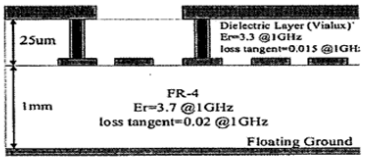
Figure 15. Glass 3D Solenoid Inductors [24]

Emerging helical inductors utilize double-side copper metallization in glass substrates interconnected with through- vias to form solenoid or daisy-chain structures. They offer excellent Q-factor, owing to the unhindered flux distribution and low dielectric loss through the structure. Realizing such via-based helical inductors using on-chip processes is not effective since the Q-factor and inductance density of helical inductors depend on the cross-sectional area, and also on the resistivity of the substrate material [28]. The ability to form through-package vias (TPVs) having small diameters, and the inherent low loss-tangent of glass substrates enable helical inductors with inductance densities comparable to that of spiral inductors, and very high Q (>60).

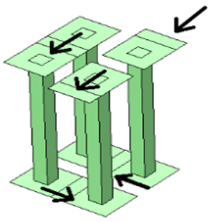
Multiple reports have demonstrated TPV-based helical inductors on glass substrates to be superior to that of spiral inductors in terms of Q [29-31]. The key considerations in the design of such substrate-embedded helical inductors are: a) TPV diameter, b) TPV filling, c) TPV pitch, d) thickness of substrate, and e) surface metal thickness. While thicker substrates enable longer TPVs, the diameter of TPVs in such substrates is limited by the aspect ratio that is supported by the TPV formation and metallization processes. Alternatively, thinner substrates enable TPVs having smaller diameter and finer pitch. Such trade-offs are a critical part of the design of high-Q helical TPV-based inductors. Various RF inductor designs and their electrical properties are summarized in Figure 16.

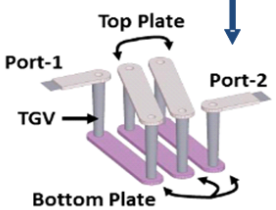






	Inductance	Size (Sq. nm)	Thickness microns	Cutoff Freq. (GHz)	Q- max
Lutz, R. D et al., [32] Spiral, RFIC	11 nH	0.04	500	4.4	11
Lee, H. H, et al., [33] Spiral, Organics	16 nH	1.29	900	4	66
Lee, S. H, et al., [34] Spiral, Organics	3.6 nH	0.72	1000	10	100
Sridharan, V, et al., [35] TPV inductors, Glass	0.4 nH	0.25	300	>14	70
Kim, J, [36] TPV solenoid, Glass	4.5 nH	~0.24	250	>2.5	80
Lai, WC et al., [37] TPV Helical, Glass	2.3 nH	0.58 (0.68 x 0.85)	150-200	10	69
Nanoinductors (projected)	10-20	<0.5	20	2	70





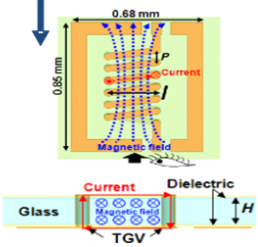


Figure 16. Summary of RF inductor designs and properties [32-37].

Miniaturization of RF passive components such as filters, diplexers, couplers, matching networks, antennas and EMI isolation structures needs materials with higher permittivity and permeability, along with stability in dielectric and magnetic properties with temperature and frequency. Traditionally, RF components were mostly confined to thick-film LTCC owing to their low loss, stable properties, and partial integration capability, although the end-systems with these technologies are still bulky. Polymer dielectrics were subsequently utilized as multilayered organic substrates, to provide the benefits of low-cost manufacturing and total integration capabilities with the rest of the polymer-based systems in spite of their low permittivity and poor tolerance leading to large component designs. Nanoscale dielectrics are suitable for miniaturized RF capacitors and other RF components. Nanomagnetics and nanomagnetodielectrics are seen as the next stage of evolution in RF components, beyond LTCC, polymer dielectrics and inorganic thin films. These materials show high permeability in microwave frequencies while also retaining low loss compared to microscale materials. By designing the nanomagnetic structure, its properties can be tuned for variety of applications, two of which are briefly introduced here.

Miniaturization of magnetic components such as inductors faces several performance trade-offs associated with frequency stability and Quality factor. A variety of inductor topologies have been explored to miniaturize inductors while retaining high performance. Inductor designs are broadly classified as spiral and helical types. Spiral

inductors utilize coils on a plane resulting in out-of-plane magnetic flux [41]. Inductance density is typically enhanced by increasing the number of turns, however, at the expense of the coil resistance and capacitive coupling between the turns, which degrade the Quality factor (Q). Incorporation of magnetic materials as inductor cores can enhance the inductance density and reduce the need for the number of turns, thereby increasing the Quality factor. For RF inductors, magnetic materials introduce losses which invariably degrade the Q. Most magnetic materials also do not show frequency-stability beyond 1 GHz. This section reviews material options and design advances to enhance inductance density and Q with nanomagnetic films.

Metals such as Co, Fe, and their alloys have high saturation magnetization and permeability. Such materials are successfully processed at microscale for integrated inductors because of their easier processing with electroplating. A thin layer of isolation is used between the core and the windings. However, these are not suitable for applications beyond 10 MHz because of their high electrical conductivity that leads to eddy current losses. These are mostly suitable for low-frequency (<5 MHz) power inductors.

Ferrites are based on oxides of these metals and have higher electrical resistivity, thereby are more suitable for higher frequencies. Spinel ferrites (e.g., $NiFe_2O_4$, Mn-Zn- and Ni-Zn-ferrites) are extensively used in power converters because of their high resistivity, resulting in high Q factors at moderate frequencies of 100 kHz to 10 MHz. However, for RF applications, ferrites suffer from several major disadvantages, including low saturation magnetization, and poor frequency response of magnetic properties due to

their strong relaxation behavior. The tradeoff between high permeability levels and operation at high frequencies is given by Snoek's limit [42].

$$(\boldsymbol{\mu_r - 1})\boldsymbol{F_{res}} = \left(\frac{\boldsymbol{\gamma}}{\boldsymbol{3\pi}}\boldsymbol{4\pi M_s}\right) \quad \text{Equation (1)}$$

For soft magnetic thin films with uniform uniaxial in-plane anisotropies, a modified law, known as Acher's limit, is applicable:

$$(\boldsymbol{\mu_r - 1})\boldsymbol{F_{res}^2} = (\frac{\boldsymbol{\gamma}}{\boldsymbol{2\pi}}\boldsymbol{4\pi M_s})^{\boldsymbol{2}} \quad \text{Equation (2)}$$

Where F_0 is the FMR frequency and γ is the gyromagnetic factor. Thus, a high saturation magnetization ($4\pi M_s$) ensures high permeability at elevated frequencies of operation. Although certain hexaferrite films with GHz frequency-stability are emerging, they have inherent low permeability because of the Snoek's limit [43] and are used mostly for non-reciprocal components such as circulators and isolators.

Magnetic nanocomposite materials are comprised of nanoscale magnetic particles in an insulating matrix. For nanocomposites, the FMR is related to the effective field anisotropy, and is represented as [39]:

$$\frac{\boldsymbol{\omega_{FMR}}}{\boldsymbol{\gamma}} = \boldsymbol{H_{eff}} \quad \text{Equation (3)}$$

where F_{res} (FMR) is the resonance frequency, γ is the gyromagnetic ratio and H_{eff} is the effective field anisotropy. The frequency stability for metal-nanocomposites is in multi GHz range. The FMR is estimated to reach 4 GHz for cobalt or iron nanocomposites while that for nickel is 2 GHz. The peak broadening with nanoparticles creates high

losses even at lower frequencies [44]. Further, the nanoparticle size demagnetizes the particles resulting in permeabilities of 5-10, unless they are exchange-coupled. Such exchange coupling is shown to be feasible with sputtered nanocomposite or nanolaminate films. The frequency-stability of loss tangent with micro- and nanoscale composites is illustrated in Figure 17, using fundamental equations superimposed with experimental data [38-51].

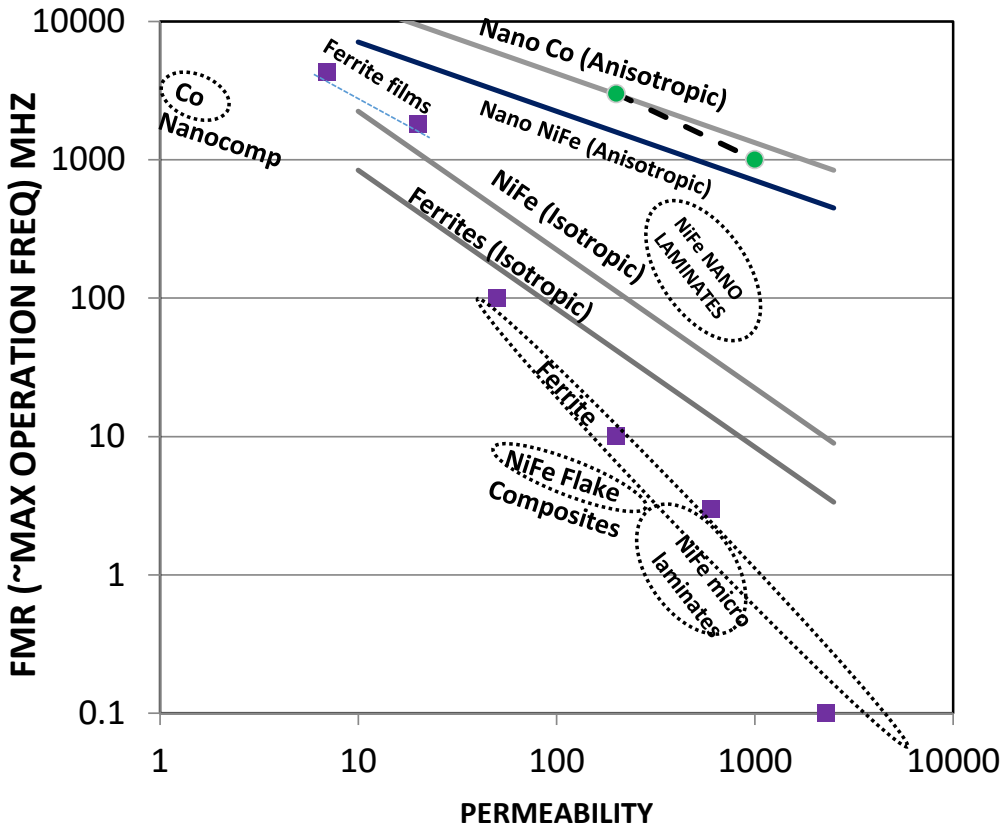


Figure 17. Permeability and frequency stability of various magnetic materials.

Higher permeability in magnetic nanocomposites at microwave frequencies can be achieved by reducing the particle size and the separation between neighboring metal

particles down to the nanoscale, which leads to novel magnetic exchange coupling phenomena [45]. For example, Co- or Fe-based nanocomposites show much higher permeability and frequency stability at microwave frequencies than those obtained from the bulk Co or Fe metal or their microscale composites [46]. Within the characteristic exchange length l_{ex}, the nanomagnetic domains interact through exchange-coupling across different grains [47]. The exchange interaction in nanocomposites also leads to the cancellation of magnetic anisotropy of individual particles and the demagnetizing effect, leading to improved soft magnetic properties. Because of the nanosized-metal particles, the eddy currents produced within the particle are also negligibly small, leading to much lower loss for nanocomposites, compared to that of conventional microsized ferrites and powder materials.

Nanomaterials also take advantage of the uniaxial magnetic anisotropy for higher frequency stability and current-handling. Nanolaminates can increase the roll-off frequency to beyond 1 GHz [48]. The superiority of anisotropic nanometallic materials is illustrated in Figure 17, where both the permeability and frequency-stability are enhanced compared to isotropic films.

Thermal Management

An RF power amplifier (PA) converts a low-power RF signal into a high-power signal, typically for driving the antenna of a transmitter. However, even an RF PA with a very good power efficiency utilizes less than half of the total power supplied. More than 60% of the supplied power is dissipated as heat, depending on the PA IC design options, cost and performance. With the trend to increased miniaturization with higher component densities, the heat dissipation of PA becomes a major bottleneck for system performance and reliability. As the power density or the amount of heat concentrated at the local area across the chip further escalates, the performance of sensitive components such as matching networks that are in proximity with the PA die also gets affected. Therefore, more effective ways to dissipate the heat from the PA hotspot down to the PCB need to be developed.

High peak power and high efficiency RF and mm-wave ICs such as GaN and GaAs require very high-power efficiency and ultra-low loss packages that must also deal with the extremely high, localized heat generated by the amplifiers. The use of hygroscopic and low-temperature epoxy molding compounds has limited the use of QFN and lead frame packages to lower power levels typical of low-noise amplifiers. There is a critical need for new package materials and processes that can effectively meet the electrical, thermal and thermo-mechanical requirements of future high power RF IC modules for high volume applications. High-power RF ICs have been traditionally packaged in bulky ceramic and metal packages, with outstanding reliability. The ceramic packages, however, suffer from miniaturization limits as well as high cost coming from

small panel sizes used for fabrication and assembly. A variety of fan-out or embedding technologies are emerging to further enhance the performance and form-factors of packages.

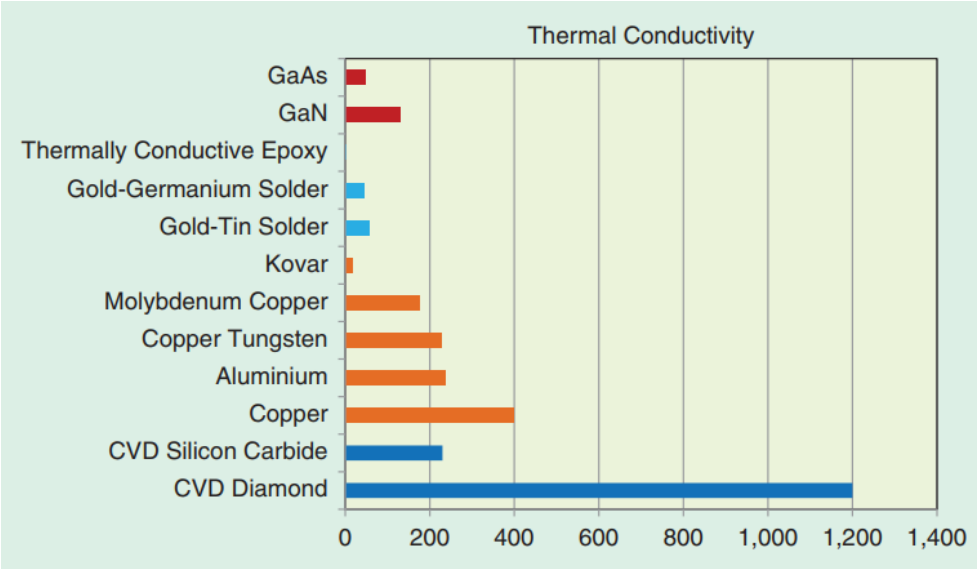


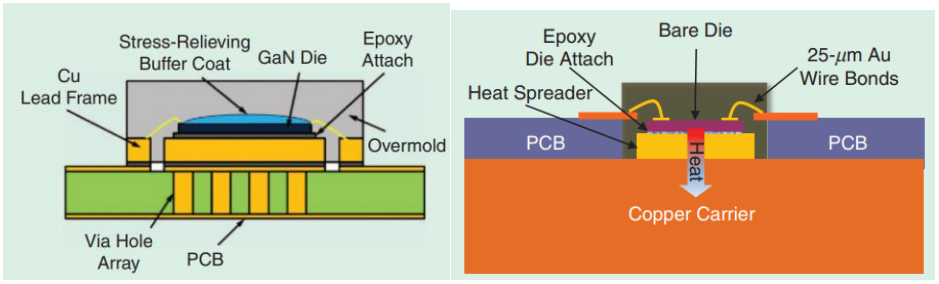
Figure 18. Thermal conductivities of PA packaging materials [52].

Advances in thermal management with material enhancements were reviewed by K. Samanta [52]. Thermal conductivites of typical PA packaging materials are compiled in Figure 18. These include both traditional and emerging strategies for wide-band and high-power RF components that operate with the highest performance and also meet the reliability targets. Several solutions are being explored for cooling high-power density RF devices. These are:

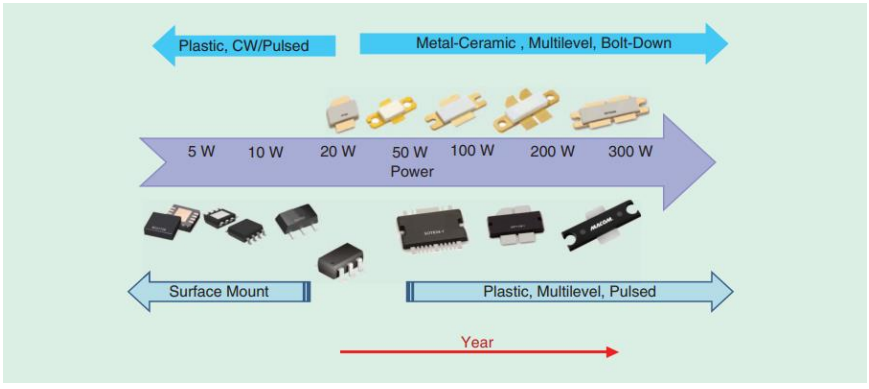
- High-temperature over-molded plastic (OMP) packaging with integrated heat spreaders and heat-capacitor using phase change materials (PCM),

- Hybrid ceramic-metal air cavity packages with direct die-attach to copper heat spreaders
- High-temperature-molded planar and multilevel plastic packages
- Integration of active cooling techniques using microfluidics.
- Embedded packages with integrated thermal structures

Examples of these are illustrated in Figure 19. The article also reports advanced high-temperature-molding compounds, CTE-matched epoxy, and TIMs that allow packaged GaN parts for achieving state-of-the-art power density (to 300 W) and efficiency, with low-cost materials and assembly techniques.



(a) (b)



(c)

Figure 19. (a) SMT plastic power package, (b) high-temperature molded plastic package and (c) evolution of packages from SMT to metal-ceramic air cavity packages and molded plastic packages.

In order to improve the thermal performance and electrical grounding, Nelson at el. [53] considered several factors such as materials selection, mechanical design parameters, assembly materials and technologies, and inspection tools for reliable solder joints with low thermal resistance and a low source impedance for enhanced RF performance. In a detailed parametric study, the heat-dissipation characteristics of different heat sink materials such as copper and aluminum are also compared. Their results demonstrate the superiority of copper for heat dissipation. In addition to that, the drop in junction temperature by about 10°C to 20°C caused a doubling of the Mean-Time-To-Failure (MTTF).

Another technique to cool PA die is the introduction of a heat-capacitor such as PCM, which absorbs heat through a phase transition in the material. Hoffman et al. [54] performed a detailed thermal analysis with several materials and also studied their performance with locational variation. Eicosane paraffin wax was used as PCM because of its high latent heat capacity and melting point of 36°C. The latent heat storage of the PCM was experimentally determined to be 50.5kJ, which is higher than the design specification of 48.7kJ. Thus, during the phase transition region, the module was able to maintain a constant temperature over defined periods of continuous operation for up to 30 min.

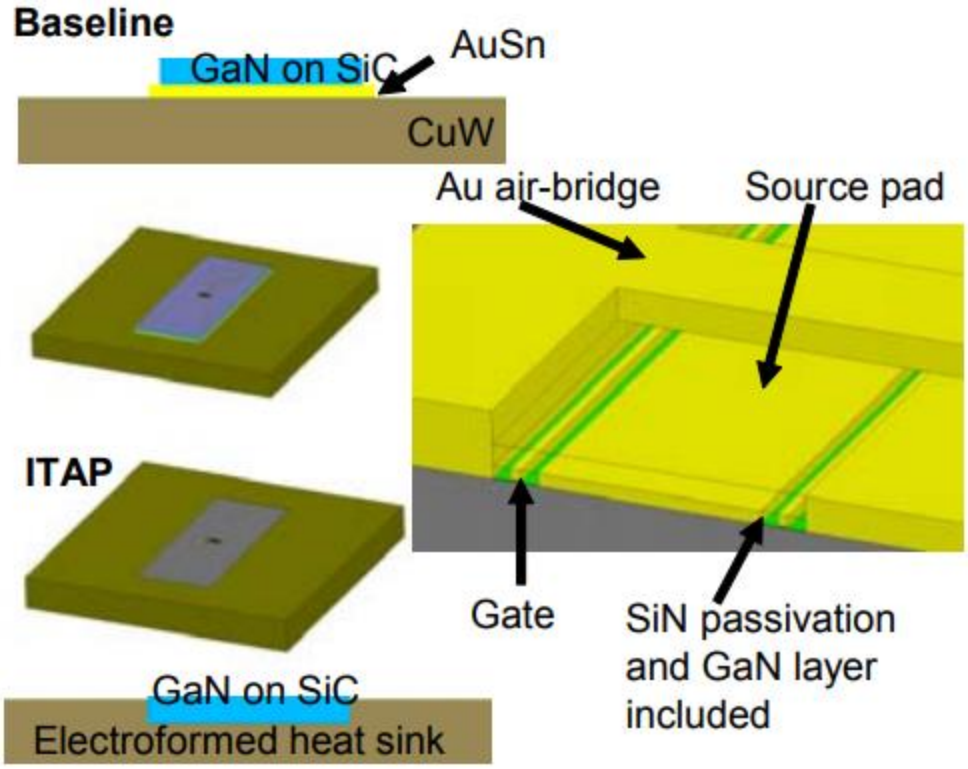


Figure 20. Copper electroforming on die backside.

Alternative techniques such as heat sinks are also commonly used, depending on thermal budget and external conditions surrounding the chip [55]. Lastly, another approach based on active heat sink antenna [56] utilizes the antenna for multiple purposes, not only utilizing it as a transmitter but also for cooling. In the suggested structure, the PA circuit is connected to the wire-fed patch antenna by a conducting cylinder, which acts as a heat spreader and also gives a path to the ground plane.

Recent trends in RF front-end module incorporates innovative thermal structures associated with the high-power density of GaN devices. A. Margomenos et al., [57][58] demonstrated a wafer-level package approach that provides an innovative method to simultaneously package, cool and interconnect RF front-end components including GaN IC. The suggested cooling technology in this paper is referred to as substrate Integrated

Thermal Array Plate (ITAP) as illustrated in Figure 20. ITAP is achieved by forming a composite substrate utilizing double-side polished alumina wafers with embedded electroformed heat spreaders and through substrate vias. GaN X-band power amplifier and a Tj evaluation circuit show improved performance in output power with ITAP, compared to conventionally mounted components using silver epoxy or AuSn solder. (1.42x and 2x better respectively). Pipe methods utilize micro-scale heat pipes to extend the heat removal path. In a detailed analysis by Langari et al., almost 26% decrease in maximum junction temperature was achieved with such cooling [59].

Active cooling with microfluidics:

Heat from RF front-end modules can be dissipated with microfluidic cooling technology utilizing microchannels that are micromachined in a copper carrier as illustrated in Figure 21. O. Chlieh et al. [60] rigorously analyzed the impact of microfluidic cooling [61][62] on the electrical performance in output power and power added efficiency (PAE) of GaN-based power amplifier module. According to this paper, heat removal is achieved by the motion of distilled water below the GaN die, while tuning is achieved by swapping air and acetone inside the source and load matching network microchannels. Additionally, Hanju Oh et al. [63] applied this microfluidic cooling technology to verify the electrical characteristics of Through-silicon-via (TSV). It is reported that the capacitance and conductance of the TSVs increase at high frequency as the micropin-fin diameter decrease at a fixed TSV pitch.

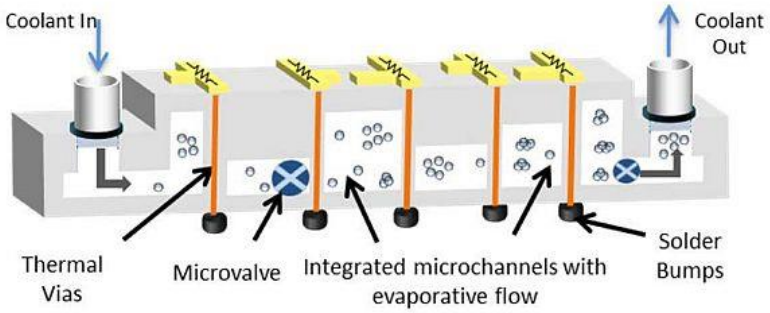


Figure 21. An example of microfluidic cooling technology

For high-power applications in processors and servers, cooling fans [64] are also used in combination with heat sink to maximize heat-transfer efficiency as illustrated in Figure 22. Microfluidic channel cooling [65] is another convective technology where water flows in a closed loop underneath the chip area to exchange the heat along its way. A recent analysis by Zhimin Wan et al. showed a temperature drop of 18.8°C and 66.2% reduction in leakage current with microfluidic cooling compared to natural air cooling, at a heat flux of 34.5 W/cm^2. With regards to spray cooling method [66], the system contains a silicon micro-machined nozzle, which injects a constant flow of fluid, at ~0.15 l/min, onto the heated RF PA die. With this approach, the junction temperature and the total thermal resistance were estimated to reduce from 214°C to 115°C, and from 1.5° C/W to 0.6 °C/W respectively.

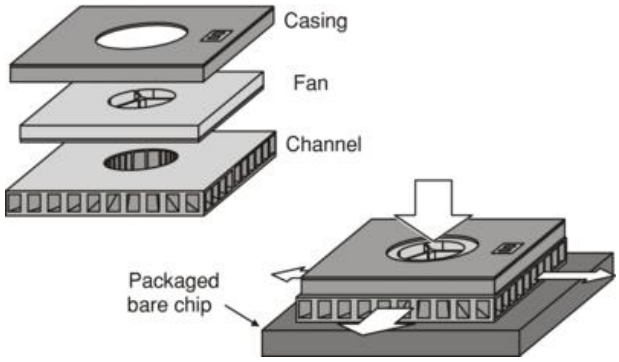


Figure 22. An example of microelectronics fan cooling

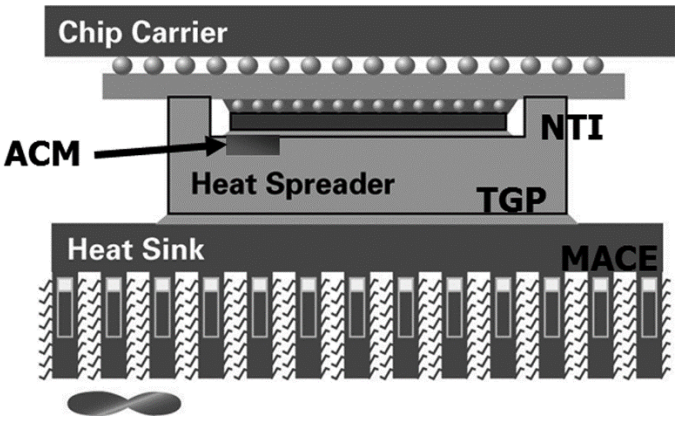


Figure 23. An example of embedded package cooling [Avram Bar-Cohen et al]

Cooling of embedded packages:

Device-embedding in laminate-glass enables doubleside cooling. Top-side cooling is facilitated by copper via structures and heat-spreaders, while the backside cooling is facilitated either by access to the die surface for either galvanic (plated copper) contact to a copper heat-spreader or die-attach as illustrated in Figure 23. The material properties of several die-attach options are shown in Figure 24. Such passive cooling is highly preferred because of its fewer process constraints and design flexibility. GT-PRC has been pioneering several die-attach options to copper. These include enhancing solders

with metastable solid-liquid interdiffusion (SLID) based interconnections, hybrid metal-polymer adhesives with sintered paste, and novel nanocopper foams for low-temperature direct copper interconnections. These solutions will be optimized to simultaneously achieve superior thermal conductivity, stability beyond 200°C and low-temperature processing.

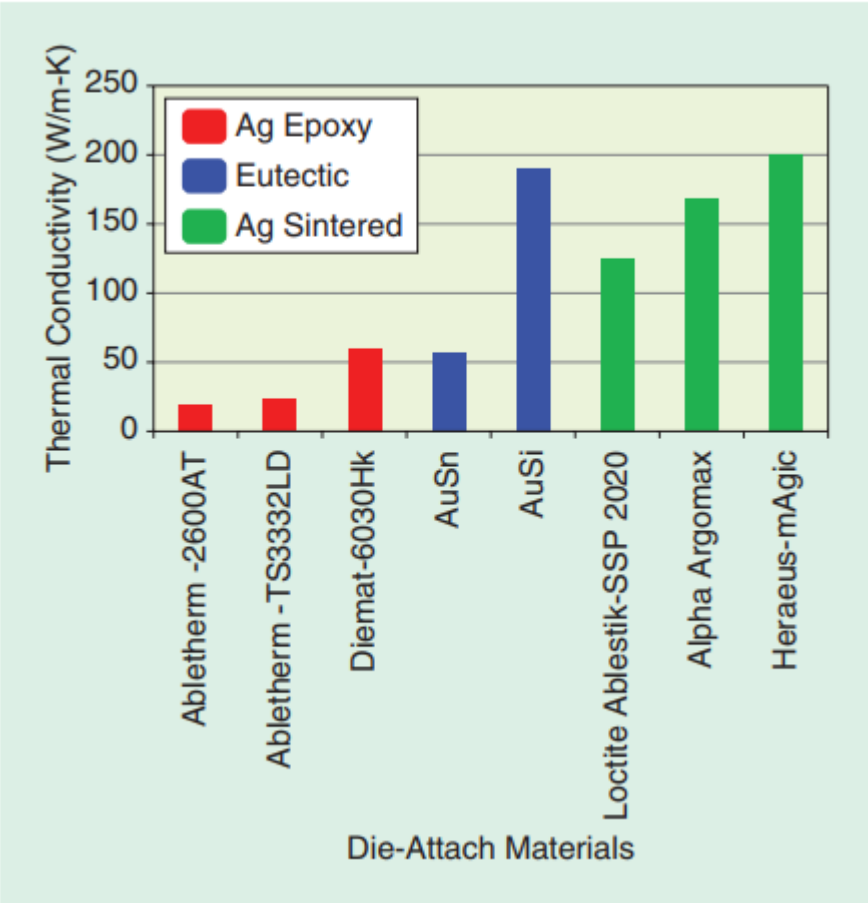


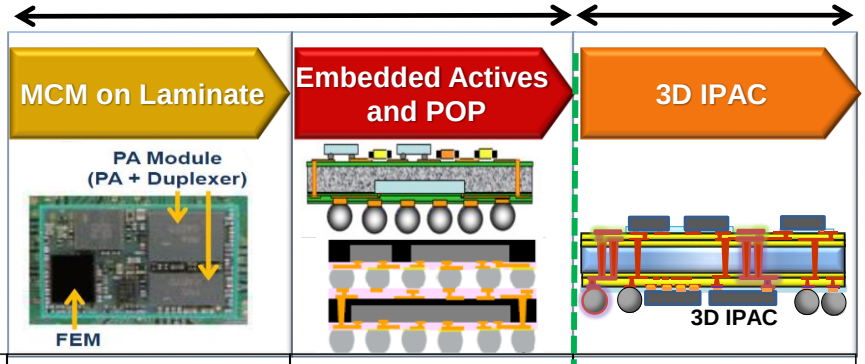
Figure 24. Thermal conductivities of various die-attach materials.

Low-cost laminate-glass substrate technology, pioneered by Georgia Tech. PRC, is emerging as an ideal platform for RF packaging because of its low loss, dimensional stability for precision and impedance-matched RF transitions, and ability to support

thinfilm passives, while also enhancing the interconnection reliability because of the low coefficient of thermal expansion (CTE) of the glass core in the package. The high stiffness and glass transition temperature also suppresses package warpage. Fan-out embedding of devices in laminate glass panels (also referred to as panel glass fan-out) brings additional advantages from ultra-short vertical interconnection lengths for lowest parasitics. However, the low thermal conductivity of glass creates major challenges with its thermal performance. Advanced thick copper structures with glass are needed to provide thermal path in order to cool the ICs. This forms the key focus of this research and will be discussed in Chapter 4.

RF Front-end modules

RF module integration initially started with LTCC substrates because of their low dielectric loss, excellent stability with temperature and humidity and ability to form complex multilayered circuits with dozens of layers. Because of its cost and wiring density constraints, LTCC technology started to migrate to organic laminate packaging because of its lower cost and higher component density from fine-line multi-layered wiring. This RF module trend is shown in Figure 25. Organic substrates that are ~0.3-0.5 mm thick form the preferred platform for today's modules, with up to two-metal layers on each side of the core. The lines and spaces are approaching 15-20 µm with vias of 100 µm in leading-edge RF substrates [67][68]. In addition, certain inductors are embedded inside the laminate substrate. Both LTCC and organic laminate substrates co-exist in today's smartphones as illustrated in Figure 26 and Figure 27. Both LTCC and organic laminate substrates co-exist in today's smartphones.



Technology	2D or MCM	Embedded die and POP	3D
Substrate	▪ LTCC/Organic; 0.3mm ▪ 15-20μm L/S; 100μm via	▪ Organic; 250μm with 4-layer & embed discretes ▪ Core 50-100μm; ▪ Build-up: 15-20μm	▪ Ultra-thin glass ▪ 5-15 μm build-up
Components	SMT discretes:0.15-0.25mm	Embedded & SMT Discretes	Thinfilms: 5-10 μm
Interconn. and Assembly	Reflow (Ht: 150 μm)	Reflow or Chip-first	Cu, SLID: <10 μm
Size	10 mm^3	5-10 mm^3	1-3 mm^3
Shielding	Package-level; Thick Cu	Limited IC level, Thick Cu	Component level; Thin
Component density	Low	Medium	High

Figure 25. RF module trend from 2D laminates to embedded and 3D IPAC or fan-out packages.

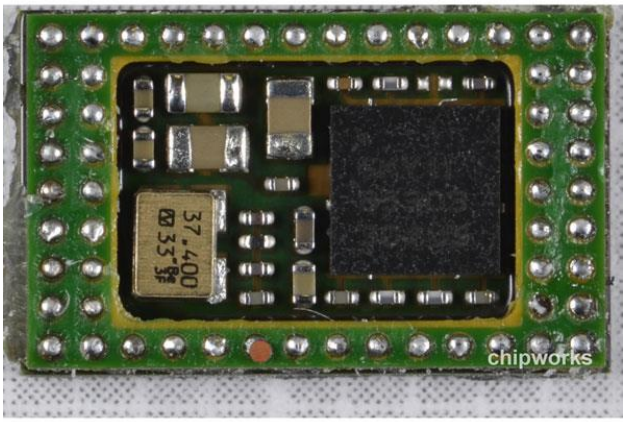


Figure 26. An Examples of Wireless module with embedded components

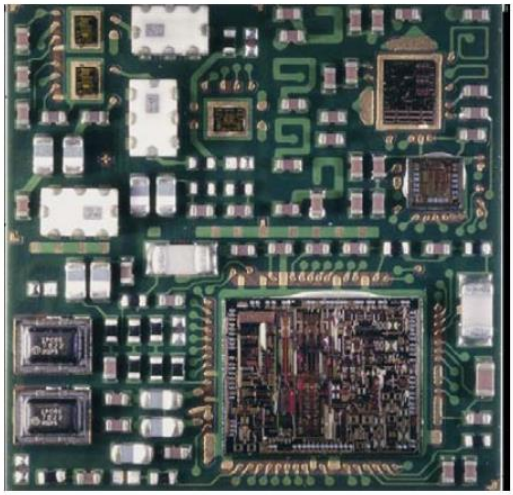


Figure 27. Laminate-based RF SiP example (Courtesy: Skyworks)

Dong-Ho Kim et al [69] demonstrated a novel integrated dual-mode RF FEM for Wi-Fi and Bluetooth application realized by LTCC technology [70]. All the passive components in the filters were fully embedded in the substrate as illustrated in Figure 28. RF FEM filters were achieved with 3 PIN diodes which are located at each output port to select Tx/ Rx. The overall size of the dual-mode RF FEM is reported to be 3.0mm x 3.0mm x 0.308mm. Continuing the trend to embedded passives, Gye-An Lee et al [71] also designed and demonstrated novel compact embedded super-diplexer for quadhand GSM RF system for its low cost laminates and feasible replacement of discrete LTCC low-pass filter and diplexer.

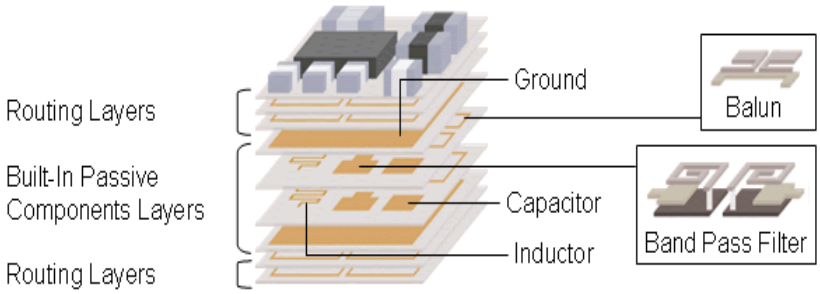


Figure 28. An example of LTCC module with embedded passive Technology

(Courtesy: Kyocera)

Emile Davies-Venn [72] has demonstrated miniaturized RF Transformer-based Baluns, which are composed of package-embedded symmetric differential inductors and capacitors, for WLAN modules in organic package substrate. Along with embedded passives, this package also integrates switch IC for Tx/Rx, Tx Balun, and Rx band-pass filter into the molding package [73]. The molding process is performed with lamination and patterning, in contrast to normal leadframe packaging of ICs. This process, therefore, has the advantage of short interconnection length from from chip to chip, compact size, and low cost in comparison to packages using wire-bonding.

Although, low-loss organic substrates have gained in popularity for RF applications, their poor dimensional stability and warpage, as well as their moisture uptake pose challenges for miniaturizing RF modules or subsystems [6][7]. The evolution of fan-out and embedded wafer level ball grid array package technologies (eWLB) further enhanced the performance or RF packages with reduced parasitics and footprint by eliminating the use of wire bonding, thick substrates and solder interconnections.

Double-sided multiple redistribution layers are formed to fan-out the transceiver input and output signals and through-mold vias are employed to realize the vertical interconnections.

Panel-based embedding is emerging as another compelling alternative to wafer-level fan-out [8-13]. S. Sitaraman [67] demonstrated Wireless Local Area Network (WLAN) RF front-end module incorporating the smallest, high performance band-pass filter (BPF), which has a footprint of 1mm × 1mm × 0.05mm, a low-pass filter (LPF) on a 110μm organic substrate with chip-last embedded actives and thin-film passives as illustrated in Figure 29. The assembled multi-dies include a power amplifier (PA) die, a switch die, and two low-noise amplifier (LNA) dies, integrated with a BPF and a low-pass filter (LPF). The gain of PA is around 10.8 dB at 2.4GHz while the path between the antenna and the amplifiers is also characterized to have a loss of 3dB. Further, ultra-miniaturized 3D Integrated Passive and Active Components on ultra-thin glass substrate (100 μm) was demonstrated along with small TPVs and fine-line RDL [68]. The substrate was fabricated using low-cost panel based processes and then assembled onto PCB through BGA interconnections. The simulation and measured data are reported to be in good agreement with low loss due to inherent excellent glass properties.

Figure 29. Multi-Die Embedded WLAN RF Front-End Module with Ultra-miniaturized and High-performance Passives (Courtesy: S. Sitaraman)

CHAPTER 3

Ultra-thin High-Q Inductors

Embedded inductors in ultra-thin glass substrates were modeled, designed, fabricated and characterized. Traditional spiral inductors can achieve high inductance density by winding copper traces as 2D coplanar or 3D multilayer coil structures, while achieving relatively good Q factor (~40) by designing with the proper ratio of line width and spacing. Despite the ease in controlling the inductance density and achieving adequate Q factors for certain RF applications, 2D inductors still face trade-offs in simultaneously achieving high Q and inductance density because the inductance density is severely compromised with large and thick metal structures.

In order to achieve higher Q factors, it is required to have more induced magnetic flux while keeping the resistance as low as possible. Through-Package-Vias (TPVs) with 100 μm diameter have much more surface area than conventional trace-based inductors. Thus, they can minimize the increment in resistance due to skin effect as the operating frequency increases. Moreover, they reduce the eddy current loss because the larger distance between TPVs can suppress the induction of any magnetic coupling in the adjacent copper networks. Furthermore, it can utilize unused Z directional space of the packaging rather than planar area in the same level.

Various 2D and 3D topologies were explored to analyze the trade-offs in inductance density, Quality (Q) factor, size and self-resonant frequency (SRF). Single-layer spiral inductors were modeled and designed to formulate an inductor library that is

optimized for high inductance densities. The design parameters include number of turns, conductor line width and spacing, and ratio of inner and outer diameter of the spiral. In order to optimize the inductor topology for higher Q factors, various types of 3D topologies with 300μm glass were also studied through modeling, design, fabrication and model validation. Inductance densities, Q, and Self-resonance frequency (SRF) were measured for various topologies.

Materials and Inductor Structures

Spiral 2D inductors are embedded in the top metal layers above the glass surface. Therefore, glass thickness is not a critical factor for achieving high performance. The inductors are designed in M1 and M2 build-up layers connected through blind vias between them, built on glass packages, as illustrated through cross-sections in Table 5. On the other hand, 3D inductors utilize doubleside copper metallization on glass, which are connected with through-package vias (TPV) as daisy-chain or solenoid structures. The glass thickness is a key factor that determines the TPV length and inductance. Table 5 illustrates the details of cross-section with materials and their thickness for 2D and 3D inductors respectively. Material properties, such as dielectric constant, loss tangent and permeability, for each type of inductor are shown in Table 6.

Table 5. Details of material stack and thickness for 2D and 3D inductor topologies

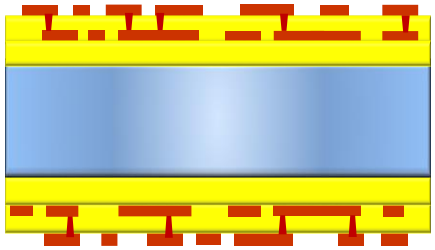
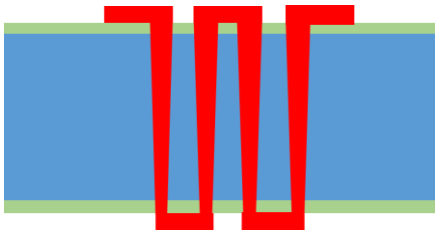
Parameter		Cross-section	Stack-up	
			Material	Thickness
2D Inductor	100µm glass		Copper (M1)	10µm
			ZS-100	17.5µm
			Copper(M2)	8µm
			ZS-100	20.5µm
			Glass (AGC)	100µm
			ZS-100	20.5µm
			Copper(M3)	8µm
			ZS-100	17.5µm
			Copper(M4)	10µm
3D Inductor	300µm glass		Copper (M1)	30µm
			GY11	20µm
			Glass (Corning)	300µm
			GY11	20µm
			Copper (M2)	30µm

Table 6. Details of material properties used for stack-ups

Inductor type	Material	Dielectric constant	Dielectric Loss-tangent	Permeability
2D inductor	ZS-100 polymer (ZEON)	3.0	0.005	1.0
	Glass (AGC)	3.2	0.0042	1.0
3D inductor	GY-11 polymer (ABF)	5.3	0.004	1.0
	Glass (Corning)	5.0	0.005	1.0

Inductor Modeling and Design

2D Spiral Inductors

The objective of this task is to find the optimal design for attaining high inductance density and Q factor. In addition, a high self-resonant frequency of more than 8GHz is needed to get the best performance at the operating frequency of 2.4 GHz. A full-wave EM simulator, Sonnet, was utilized to model the inductors. Eight spiral

inductor designs are considered, each surrounded by ground frames on both M1 and M2 layers, along with GSG probe pads for electrical characterization. Minimum line width and spacing of 10 μm are chosen as the ground rules for copper winding design. This ground rule is determined by a series of factors such as lithography tools, photoresist film, and types of mask to be used. After imposing this ground rule, several iterations of design optimization using diversified ratios of line width and spacing was performed. Optimal line width and spacing for various turns and glass thickness are obtained to get the best performance of package-embedded 2D spiral inductors with minimal skin effect, proximity effect, and parasitic capacitance. Conducting line width of 40μm and spacing of 10μm resulted in the best trade-off between inductance density and quality factor (Q).

The library designs of 2D spiral inductors is shown in Figure 30. An example of 4.5nH inductor (Design 8 in Table 7.) is illustrated with dimensional details in Figure 31(a). The perspective view of inductor design is also illustrated in Figure 31(b). The simulation results for the electrical performance of each of the 8 designs are compiled in Table 7. The optimal performance for 2D embedded spiral inductors are compiled in Table 8. These inductors are found to be suitable for high inductance density and moderate Q factors.

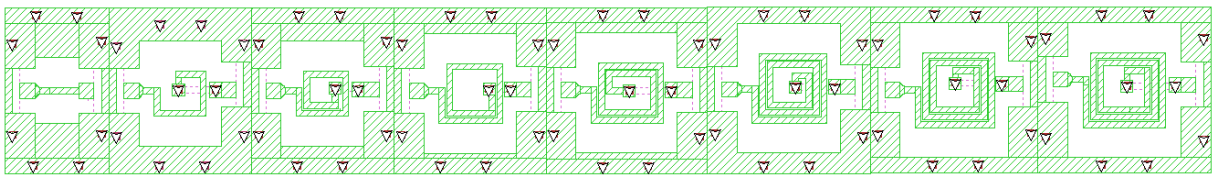


Figure 30. 2D spiral inductor library with glass substrates

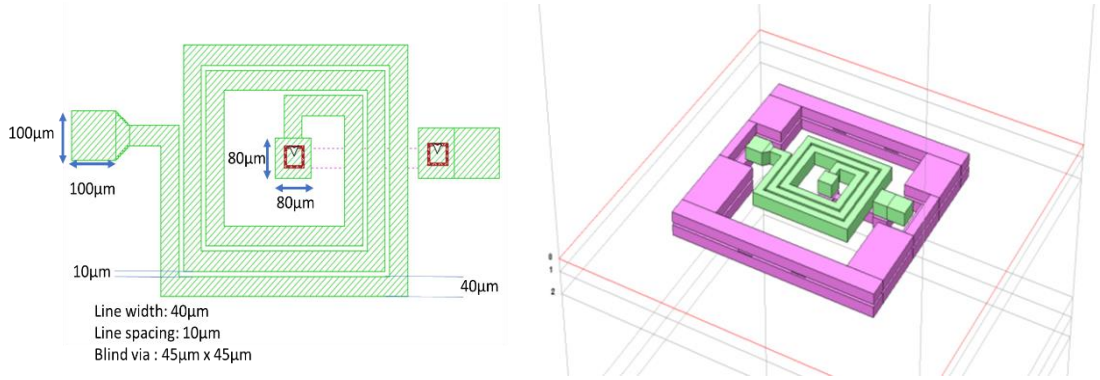


Figure 31. Spiral inductor: (a) Top view with dimensional details, (b) Overall view

Table 7. Simulation results for 2D spiral-based inductors at 2.4GHz

Target L(nH)	Area (µm x µm)	L at 2.4GHz	Q at 2.4GHz	Density (nH/mm^2)	SRF(GHZ)
Design 1	165 × 130	0.338	33.84	15.76	>15 GHz
Design 2	350 × 300	0.802	35.13	7.639	>15 GHz
Design 3	350 × 300	1.104	36.75	10.514	>15 GHz
Design 4	425 × 400	1.676	43.5	9.859	>15 GHz
Design 5	485 × 400	2.498	39.13	12.876	>15 GHz
Design 6	500 × 460	3.521	37.88	15.309	13.15 GHz
Design 7	530 × 500	4.207	39.93	15.875	11.25 GHz
Design 8	550 × 500	4.470	41.76	16.375	11 GHz

Table 8. Optimal performance for 2D embedded spiral inductors

Parameter	Specifications
Operating frequency	2.4GHz
Highest Inductance	3nH
Tolerance	5%
Inductance density	10nH/mm^2
Q factor at 2.4GHz	40
Self-Resonant frequency	>8GHz

3D Daisy-chain and Solenoid Inductors

Two types of 3D topologies with TPVs were considered: daisy-chain inductor, and solenoid inductors, as demonstrated in Figure 32 and Figure 33 respectively. These topologies utilize through-package-vias, which has advantages such as larger copper volume for lowering inductor resistance. The impact of design parameters such as number of turns, TPV pitch, aspect ratio (via height: via height) and copper thickness on inductance density, Q and SRF are studied.

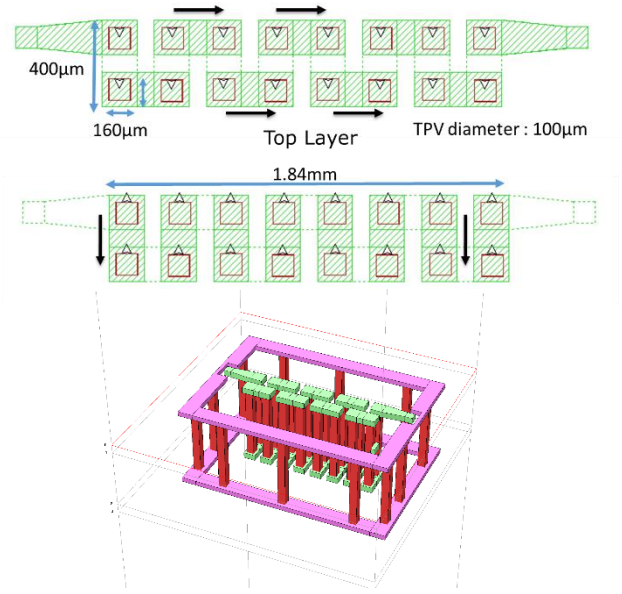


Figure 32. Daisy-chain Design: (a) Top view with dimensional details, (b) Overall view

Daisy-chain inductors, shown in Figure 32(a), comprise of two metal layers on top and bottom of glass substrate, which are connected with TPVs. The pad size for TPVs is 160µm by 160µm, and the diameter of TPV is 100µm. The current flows through both top and bottom layers. Its direction is guided with black arrows in the figure. The overall size of this inductor is 1.84mm by 0.4mm. The overall view of daisy-chain inductor is illustrated in Figure 32(b).

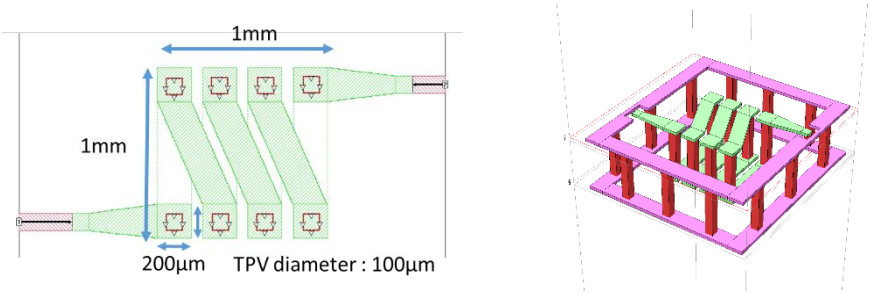


Figure 33. Solenoid Inductor Design: (a) Top view with dimensional details, (b) Overall view

Solenoid inductors offer several structural advantages in enhancing inductance density while retaining high Q factor. In order to control the inductance density, different conductor pitches and via aspect ratios can be utilized. The design details are shown in Figure 33(a). The dimensions of TPV pad and line width are 200µm. The overall size of solenoid inductor is 1mm by 1mm. The perspective view of solenoid inductor is illustrated in Figure 33(b). The optimal design and performance specifications for 3D inductors are shown in Table 9.

Table 9. Specifications for 3D inductor

Parameter	Specifications
Operating Frequency	1GHz
Highest Inductance	3nH
Tolerance	5%
Size	< 1mm x 1mm
Q factor at 1GHz	60
Self-Resonant frequency	>3 GHz

Fabrication Process

Low-cost panel processing is developed for double-side and through-via metallization in glass substrates with high precision and tolerance. The process flow for 2D and 3D inductors is described in Figure 34. In case of 2D spiral inductors, each layer

is patterned with low-loss dielectrics (ZEON Chemicals, ZS-100), which are double-side laminated onto ultra-thin 100µm glass. For 3D inductors, 300 µm glass along with Ajinomoto dryfilm-GY11 was utilized, and outer layer of copper traces are connected through TPVs. Precise fabrication for the copper traces is critical for the correlation between simulation data and the measurements.

Direct formation of TPVs by UV laser ablation of polymer-laminated glass substrates faces challenges because of excessive damage near the entrance and exit of the vias. This damage affects the quality of copper metallization around the TPVs, resulting in low yields of the 3D TPV interconnections. An improved process using pre-fabricated through vias in bare glass, followed by polymer lamination and second via formation was developed. For this process, through-vias are first formed in bare glass panels by Corning Inc, New York. The glass panels with pre-fabricated TPVs are cleaned using organic solvents (acetone, methanol and Isopropyl alcohol) to remove residues and impurities. Following this, thin dry-film polymers with corresponding thickness for each 2D and 3D inductor are laminated onto both sides of the glass substrates. The polymer flows and completely fills the glass vias. A second laser process is then used to form smaller through-vias inside the polymer filling of the pre-drilled glass vias, creating the double-via structures. This process results in a polymer liner on top, bottom and side walls of the TPVs, simplifying via metallization and improving reliability by eliminating direct copper plating on glass surfaces.

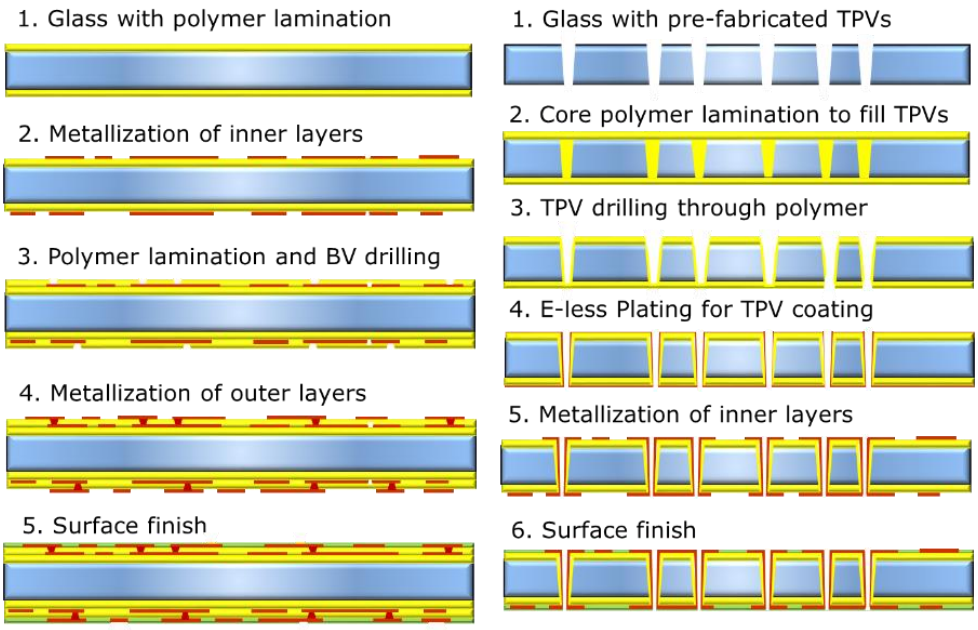


Figure 34. Detailed process flow for: (a) 2D spiral inductor, (b) 3D inductor

Two build-up metal layers are needed for spiral inductors. The build-up dielectric layers are formed from dryfilm lamination and UV laser-via drilling. Electroless plating is used to seed-metallize the polymer-coated glass surfaces. Copper circuits were formed with semi-additive patterning (SAP) process using UV dry-film lithography. The process flow for 2D spiral is illustrated in Figure 34(a). Electrolytic copper plating is used to achieve high-quality copper winding and redistribution layers (RDLs). In order to attain uniform copper thickness throughout the panel, small current (<3 amps/ft^2) is applied for a long time (> 30 minutes). However, for this lay-out, copper thickness still varied by 5-10% depending on the location of inductor coupons in the glass panel. Thus, coupons in the center of the panel were selected to examine the electrical performance of inductors because of their uniform plating. Solder mask layer was then laminated to cover the

circuitry and prevent contamination and oxidation, while only leaving the GSG pads for probing purpose.

Characterization and Discussion

2D Spiral Inductors

All the spiral inductors were designed and fabricated on ultra-thin 100 μm glass substrates with epoxy dielectrics (ZS-100). Electrical loss is minimized by the high resistivity of glass and low loss-tangent of the dielectrics. Fabricated samples of spiral inductors are shown in Figure 35.

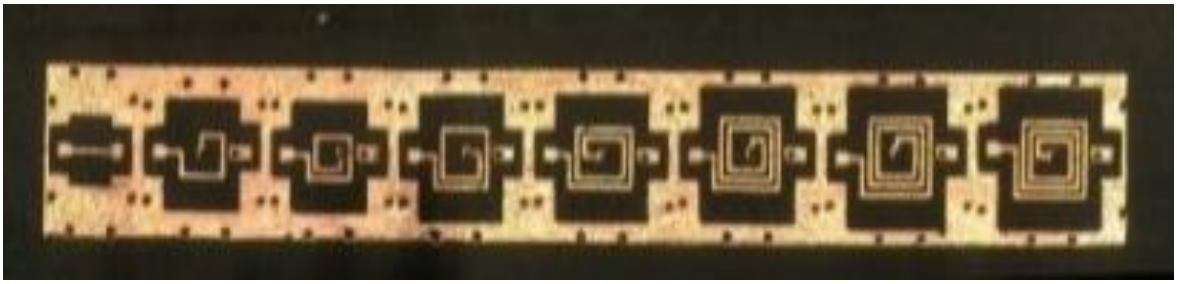


Figure 35. Fabricated 2D spiral inductor library

Electrical performance was measured with a high-precision RF GSG probe station that is connected to a vector network analyzer to extract S-parameter data in the LTE frequency band. The imported data is then converted to impedance in order to interpret them as inductance and Q factor. The measurements correlated with the designs. For Design 8 as an example, the simulated and measured inductances correlate well at 2.4 GHz, as illustrated in Figure 36. The simulated value shows 4.47 nH, while the measured inductance records 4.32 nH at 2.4 GHz. The difference between measurement and simulations is only 3.35%, which is less than 5% tolerance as per the design

specification. The simulations and measurements of inductance correlate well until 5.5GHz. Beyond 5.5GHz, the measured inductance tends to be higher than the simulated ones. The predicted Quality factor for these inductors is 41.76, while the measured Q is 40.74 at 2.4GHz, which also agrees with the simulations within 3%. In summary, 2D spiral inductors show high inductance density without much trade-offs in the Q factor at the operating frequency.

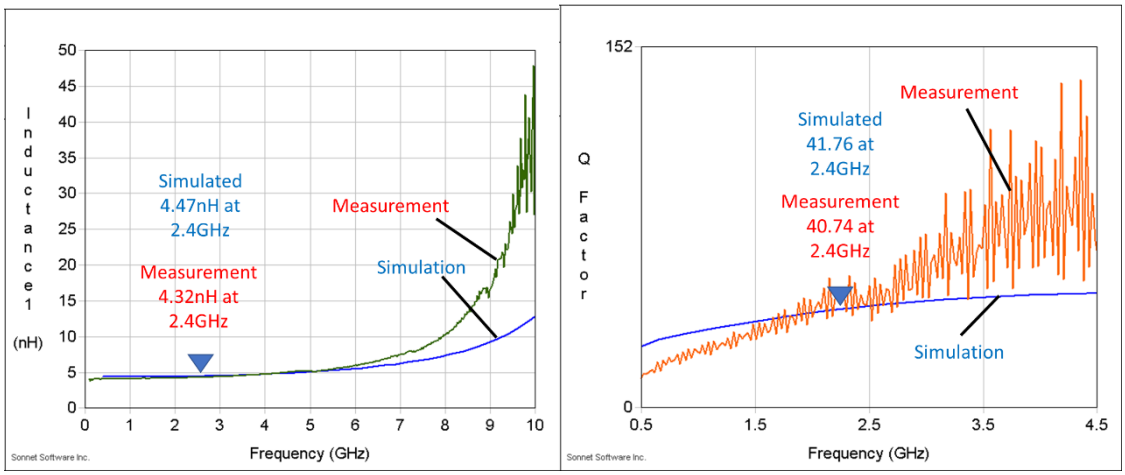


Figure 36. Measured response of fabricated 2D spiral inductors:

(a) Inductance, (b) Q factor

Several factors, as shown in Equation 4, such as mean radius of coil (r), number of turns, and depth of coil determine the inductance. Inductance increases with the size of the coil, the number of turns, and reduced spacing between the windings. The basic analytical formulations for spiral inductors are:

$$\mathrm{L} = \frac{(rN)^2}{20r+28d}, Q = \frac{2\pi f L,}{R}, and\ f_r = \frac{1}{2\pi\sqrt{LC}} \quad \text{Equation (4)}$$

L = inductance in Henries, r = mean radius of coil (cm), N = number of turns, d = depth of coil (outer radius minus inner radius) (cm), Q = quality factor, R = inductor's effective series resistance, f_r = self-resonant frequency, and C = parasitic capacitance in Farad.

The Q factor is determined by the ratio of the induced reactance and the resistance of the inductor at a specific frequency. In order to achieve high Q factor, the resistance of the inductor should be minimized while maximizing the reactance. This requires careful consideration of various contributions such as skin effect, proximity effect, loss from substrate core, leaky magnetic flux and parasitic capacitance. In particular, undesired parasitic capacitance acts to offset the reactance of the inductor. Therefore, when designing an inductor, the area in which the conductors are in parallel with each other should be minimized for low parasitic capacitance. At the Self-Resonant Frequency (SRF), the reactance from inductance and capacitance cancel each other. Inductance and parasitic capacitance determine the SRF. Larger inductor size and number of turns are required to achieve higher inductance. However, as the inductor size increases, parasitic capacitance also invariably increases due to the increase in parallel conductor branches. With increased parasitic capacitance, the self-resonant frequency is lowered, as can be verified from Design 5 to Design 8 in Table 7.

The optimal performance of spiral inductors is compiled in Table 8. The inductance densities (10-20 nH/mm^2) from spiral inductors on glass are comparable to those reported on organic laminates. Higher Q of 70-100 are reported from organic laminates [74][75] while Qs of 30-40 are also reported on glass [76]. However, the

primary advantages of glass-based spiral inductors come from its ultra-thinness and large-area panel processing. The glass packages have 100µm core and 15µm build-up layers with total thickness of 150µm. This can be extended to 50µm core without much change in the design and processing. Standard panel processes are employed to fabricate the inductors, leading to low-cost integration of both receiver and transmitter chain of LTE or WLAN modules.

3D Inductors

A completed glass panel of 3D inductors along with each inductor type are shown in Figure 37. To validate the quality of the fabricated TPVs, the 3D inductor TPVs are cross-sectioned, an example of which is shown in Figure 38. The entrance diameter of the TPVs is 120µm and the exit side diameter is 96µm. Both the entrance and exit diameters of TPVs are slightly different from the original design of 100µm diameter. More importantly, interconnections with continuous, thick and uniform copper between the top and bottom layers is the key for 3D inductors because most of the inductance arises from the TPV interconnection path, unlike with spiral inductors. Figure 38 verifies that the top and bottom layers on glass are well-connected through the conformally-plated copper in TPV. It also suggests that the polymer has flowed and coated well on the side walls of the TPVs, without which the plated metallic copper does not form a uniform layer or bond well to the TPV walls. The thickness of electroplated copper is 30µm. Although the losses decrease with increasing copper thickness, more metal volume does not significantly affect the Q factor beyond a certain point.

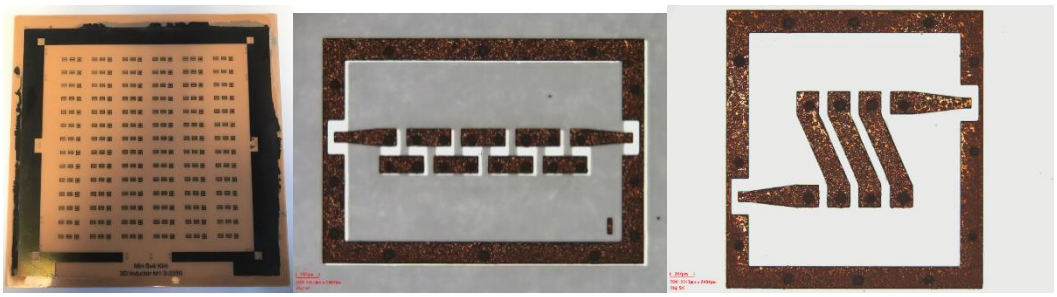


Figure 37. Fabricated 3D inductor panel and each inductor component

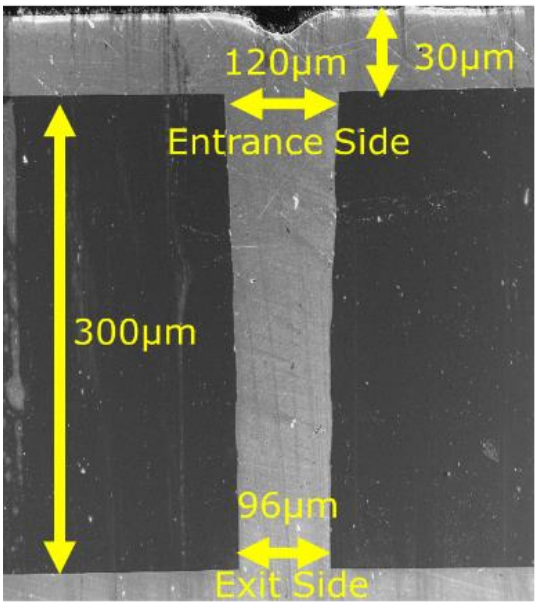


Figure 38. Cross-section of 3D inductor TPV

Equivalent circuit analysis is used to compare the daisy chain and solenoid types of 3D inductors used in this study. The equivalent circuit model for daisy-chain inductors is represented as individual via inductors that are connected to each other in series, as illustrated in Figure 39. The current that flows through the first via inductor, L_1, has no other path to flow other than through the second inductor, followed by the third one and

so on. Therefore, the via and traces form a continuous current path from one port to the other. The total daisy chain inductance can be found by simply adding the individual inductances of TPV and interconnections as shown in Equation (5).

$$L_{total} = L_1 + L_2 + L_3 + \ldots + L_n \quad \text{Equation (5)}$$

However, the above equation holds only when the individual inductors do not interfere with each other, for example, without mutual inductance or magnetic coupling between them. If the mutual inductance is positive, the total inductance of any two or more inductors connected in series is always greater than the value of the largest inductor in the series chain. If the currents in adjacent branches are flowing in opposite directions, the mutual inductance is negative and can suppress the total inductance.

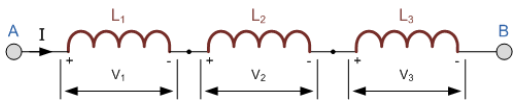


Figure 39. Equivalent circuit model for daisy-chain inductor

For 3D solenoid inductors, the mechanism that that determine the inductance are different from the daisy-chain inductors because the solenoids utilize copper winding topology rather than connection of via inductors in series. The key parameters that determine the inductance are: number of turns, cross-sectional area and length of the coil. Permeability for this solenoid is equivalent to that of air since permeability of both glass and dielectrics is equal to 1. In short, more number of turns and larger cross-sectional area with shorter length of the coils result in higher inductance density, as shown in Equation (6).

$$L = \frac{1}{l}\mu o\, KN^2A \qquad \text{Equation (6)}$$

L = inductance in henries (H), μ_0= permeability of free space = 4π x 10-7 H/m, K = Nagaoka coefficient, N = number of turns, A = area of cross-section of the coil in square meters (m^2), and l = length of coil in meters (m)

The measurement data from each type of 3D inductors is shown in Figure 40 and Figure 41. Daisy-chain inductor shows 2.115nH and Q of 72.79 at 1GHz while solenoid inductors showed 3.279nH and Q of 63.69 at 1GHz. Both inductors satisfy the specifications for Q factor, which is greater than 60 at 1 GHz, but the daisy-chain inductors recorded inductance values that are slightly lower than the target of 3 nH. The measured data demonstrates the successful metallization of 70µm diameter through-vias in the polymer inside pre-drilled 100µm glass vias in 300µm thick glass substrates. The performance of spiral and solenoid inductors is compared in Table 10.

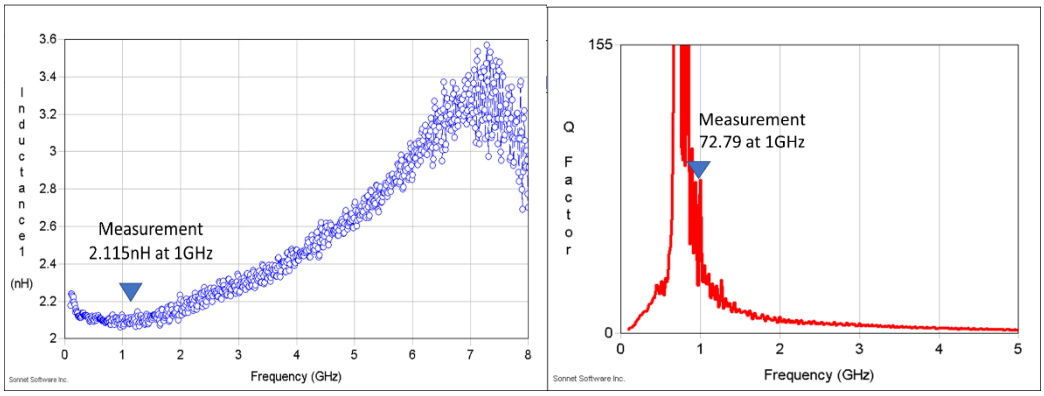


Figure 40. Measured response of inductance and Q factor from Daisy-chain inductors

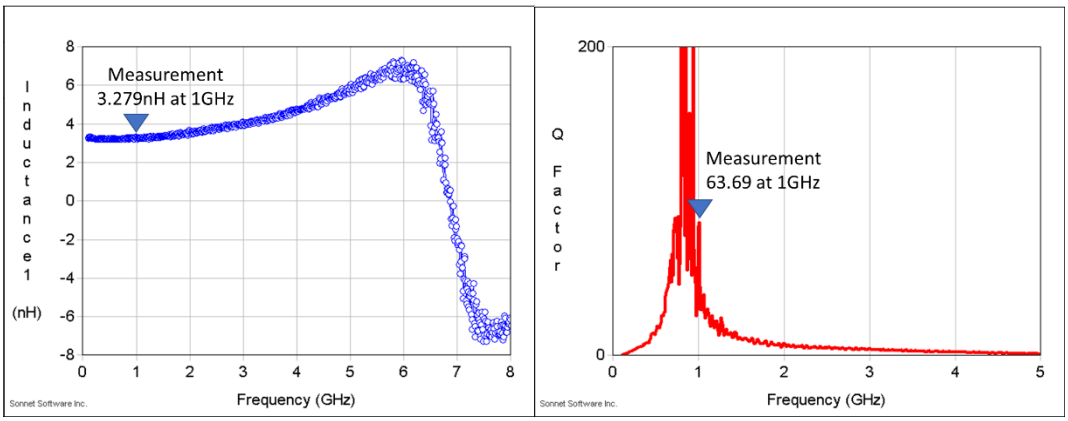


Figure 41. Measured response of inductance and Q factor from 3D solenoid inductors

Table 10. Summary of spiral and 3D inductor performance

Parameter	Spiral inductors	3D inductors
Operating frequency	2.4GHz	1GHz
Highest Inductance	4.32nH at 2.4GHz	3.279nH at 1GHz
Tolerance	5%	5%
Size	< 550µm x 500µm	< 1mm x 1mm
Q factor (at operating frequency)	40 at 2.4GHz	60 – 70 at 1GHz
Self-Resonant frequency	>10GHz	> 6 GHz

As seen from Equation (3), the inductance can be increased with more turns or larger winding loop area of the solenoid. Thicker glass directly translates to more loop area. The ability to form fine-pitch and fine-diameter TPVs, and the inherent low

dielectric loss of glass substrates enable 3D solenoid inductors with the required number of turns for achieving high inductance densities and Q-factors. Traditional thicker organic laminates limit the scaling of the TPV diameter and pitch, correspondingly lowering the inductance density. Finer TPV pitch and filled TPVs with emerging advances in glass substrate manufacturing can provide unique opportunities to enhance inductance density and Q beyond the state-of-the-art with organic laminates. The inductance densities on glass can be further improved by the introduction of nanomagnetic films with higher permeability, however, with adequate resistivity so that the eddy current losses are not dominant.

Ultra-Miniaturized High-Q Inductors With 50 Microns Glass

In order to study the impact of glass miniaturization on the electrical performance of 3D inductors, three types of 3D inductors: daisy chain, solenoid and a novel triangular solenoid, were designed, fabricated and characterized on 50 micron glass with low-loss dielectrics. Figure 42 shows the fabricated 3D inductors.

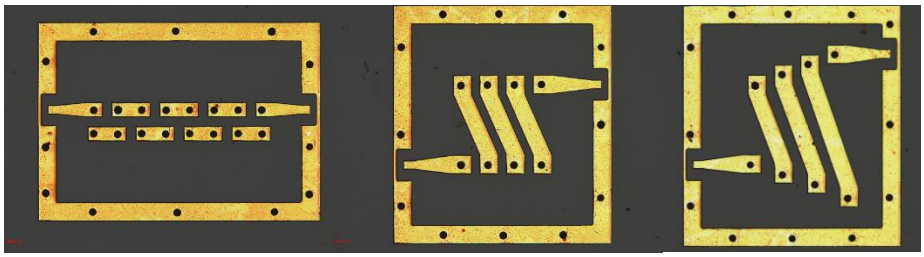


Figure 42. Fabricated 3D Inductors on 50 micron glass

(a) Daisy chain, (b) Solenoid, and (c) Triangular solenoid

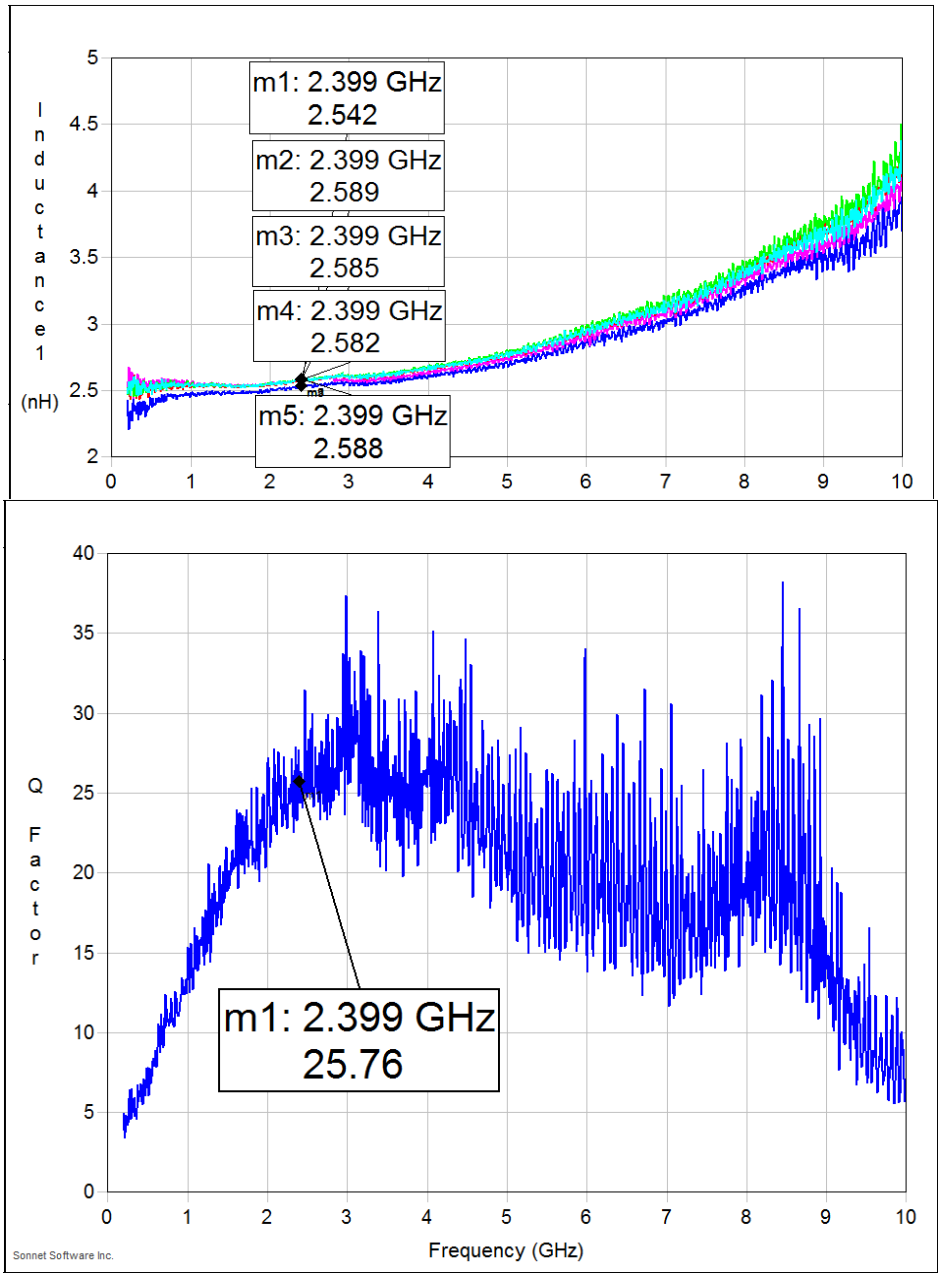


Figure 43. Electrical Characterization of daisy chain inductors in 50 micron glass;

(a) inductance at 2.4GHz, and (b) Q-factor at 2.4GHz

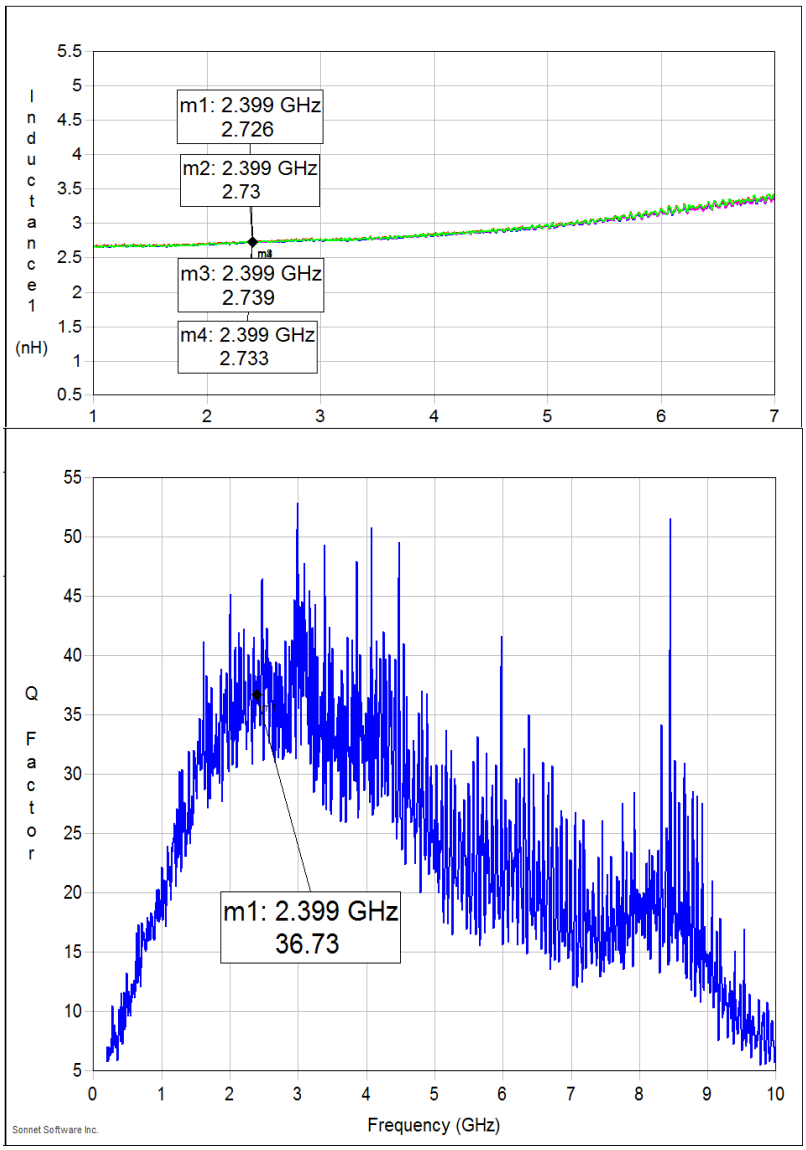


Figure 44. Electrical Characterization of standard solenoid inductors in 50 micron glass: (a) inductance at 2.4GHz, and (b) Q-factor at 2.4GHz

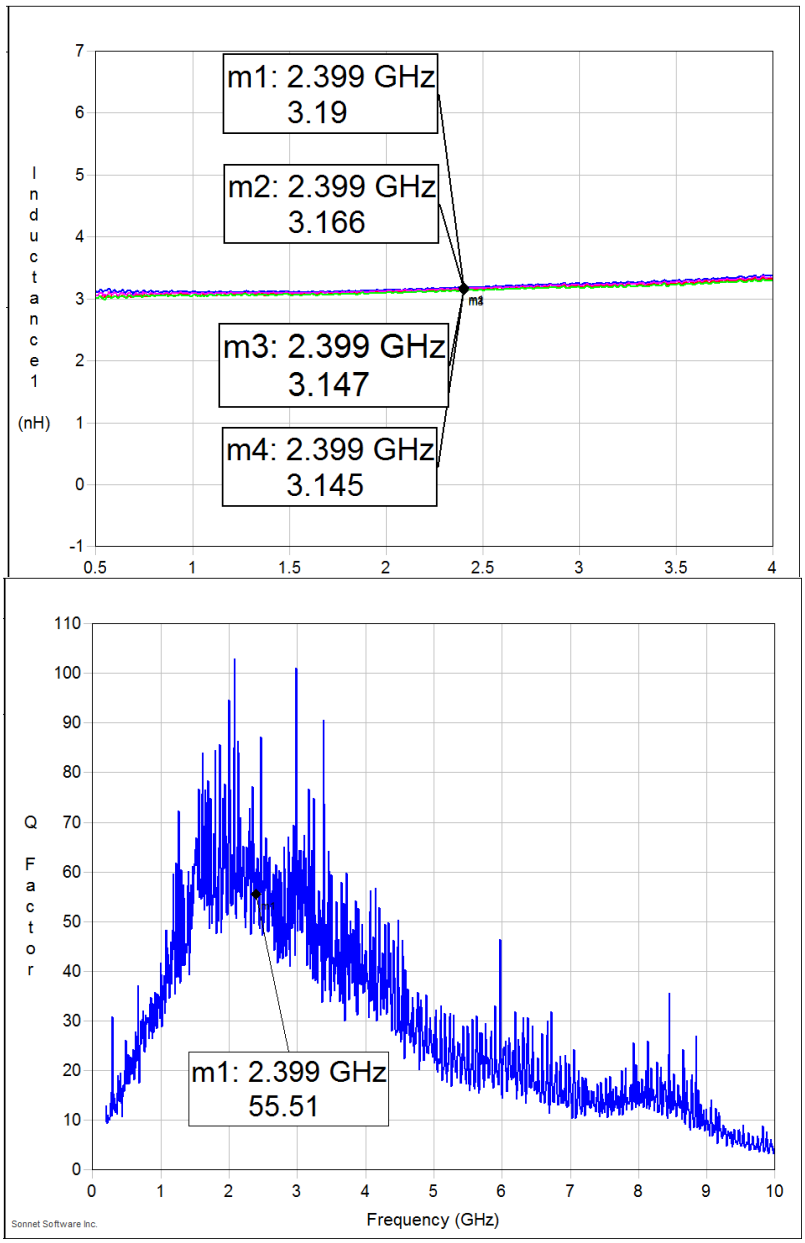


Figure 45. Electrical Characterization of triangular solenoid inductors in 50 micron glass: (a) inductance at 2.4GHz, and (b) Q-factor at 2.4GHz

Table 11. Compiled electrical performance of each type of 3D inductors

	Daisy chain	Solenoid	Triangular Solenoid
Inductance at 2.4GHz	2.58nH	2.73nH	3.16nH
Q at 2.4GHz	25.76	36.73	55.51
SRF	>10GHz	>10GHz	>10GHz

Figures 43 to Figure 45 show the measured data for electrical performance of each type of inductor, along with inductance and Q factor at 2.4 GHz. The electrical performance is also compiled in Table 11. Comparing traditional solenoid with triangular solenoid inductors, the inductance and Q factor of the triangular solenoid are improved by 15.7 percent and 51.1 percent respectively. This is because the area of the overlapped conductors is substantially reduced due to its geometrical modification. Therefore, the parasitic capacitance can be reduced to enhance the inductor's electrical performance. The data provides guidelines for low-profile air-core 3D inductors on 50 micron glass

Nanomagnetic inductors

Inductors utilize spiral or helical designs to enhance magnetic flux and inductance. Spiral inductors require large footprint while solenoid inductors require thick substrates to achieve adequate flux coupling. As such, both these designs impose trade offs in inductance density, Q, and frequency stability. Nanomagnetic films with stable and high permeability can enhance inductance density and correspondingly the Q factor.

However, nanomagnetic films suffer from two disadvantages. They have high losses beyond 1.0 GHz. They are also sputter-deposited as thin films that are less than 5 microns. Therefore, the benefits of nanomagnetic films in RF inductors are not clear. Performance improvements and trade-offs in RF inductors with nanomagnetic films are analyzed through material and component-level modeling. The inductance density and Q trade-offs with nanomagnetic films are simulated after imposing their constraints: frequency dependence and thickness of 5 microns. Both helical and spiral inductors are considered with and without the nanomagnetic films. The simulations show enhancement in inductance by 5X with mild degradation in Q for spiral inductors. However, the Q degraded more with solenoid inductors. Higher resistivity and ferromagnetic resonance (FMR) frequency are critical to improve the performance of nanomagnetic film inductors.

Solenoid inductors with 3D inductor structures utilize doubleside copper metallization on glass that are connected with through-package vias (TPV). The glass thickness is a key factor that determines the TPV length and inductance. Thicker glass is required to achieve high inductance. With the introduction of nanomagnetic films on glass, higher inductance density can be achieved with thinner glass.

Glass-based solenoid 3D inductors with doubleside nanomagnetic films were modeled for their inductance and Quality factor. A baseline solenoid inductor design was utilized with different glass thicknesses and nanomagnetic film stacks. Several different stacking scenarios were considered with different glass thickness (300 µm, 100 µm and 50 µm) and various combinations of doubleside nanomagnetic films. The inductor design parameters are shown in Table 12. The inductors have 3.5 turns. The 3D and top views of

solenoid inductors are illustrated in Figure 46. Table 13 illustrates all the properties used in the simulations. Table 14 shows the details of each material stack and their thickness

Table 12. Solenoid Inductor Design Rules

Parameter	Number
Inductor Size	1 mm x 1 mm
Turns	3.5
Copper thickness	20 µm
Line width and Spacing	200 µm, 70 µm
TPV pad	100 µm x 100 µm
TPV diameter	100 µm

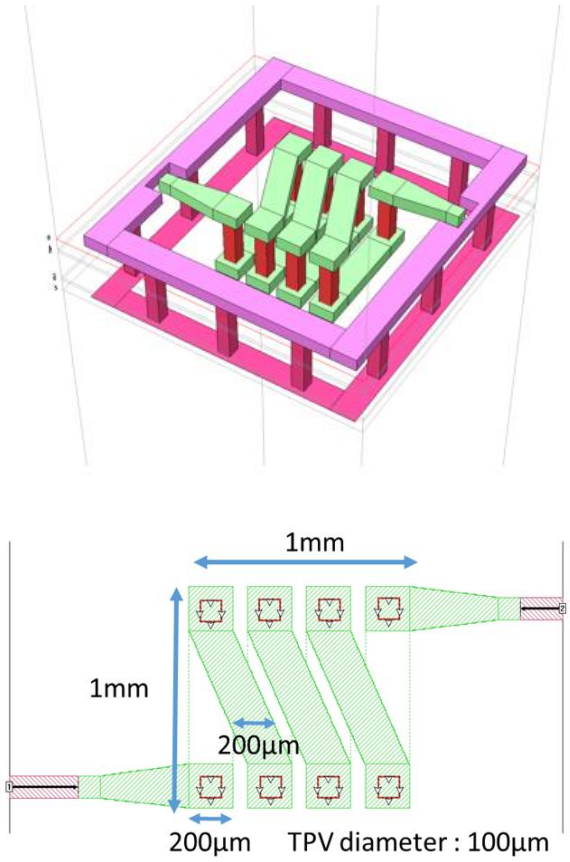


Figure 46. Solenoid Inductor Design:
(a) isometric view (b) Top view with dimensional details.

Table 13. Material properties used in simulations.

	ε_r	Tan δ (dielectric)	R (ohm-m)	μ_r	Tan δ (mag)
Epoxy polymer	3.2	0.0042	$10x10^{22}$	1.0	0
SiO_2	3.9	0.0005	$10x10^{22}$	1.0	0
Magneto-dielectric	-	-	$5.0x10^{-4}$	300	0.05
Glass	5.0	0.005	$10x10^{22}$	1.0	0

Table 14. Cross-sections for six different cases of stack-up

Cross-section			Stack-up	
Case 1	300µm glass		GY11	20µm
Case 2	100µm glass		Glass	300µm/ 100µm/ 50µm
Case 3	50µm glass		GY11	20µm
Case 4	50µm glass with double-side single stack		GY11	20µm
			SiO_2	0.1µm
			Mag. Film	50nm
			Glass	50 µm
			Mag. Film	50nm
			SiO_2	0.1 µm
			GY11	20 µm
Case 5	50µm glass with double-side double stacks		GY11	20µm
			SiO_2	0.1µm
			Mag. Film	50nm
			SiO_2	0.1µm
			Mag. Film	50nm
			Glass	50µm

Table 14 continued

			Mag. Film	50nm
			SiO_2	0.1µm
			Mag. Film	50nm
			SiO_2	0.1µm
			GY11	20 µm
Case 6	50µm glass with double-side triple stacks		GY11	20 µm
			SiO_2	0.1 µm
			Mag. Film	50 nm
			SiO_2	0.1 µm
			Mag. Film	50 nm
			SiO_2	0.1 µm
			Mag. Film	50 nm
			Glass	50 µm
			Mag. Film	50 nm
			SiO_2	0.1 µm
			Mag. Film	50 nm
			SiO_2	0.1 µm
			Mag. Film	50 nm
			SiO_2	0.1 µm
			GY11	20 µm

Simulation Results and Analysis: Table 15 compiles the simulation results for inductance and Q factor at 1GHz, along with the self-resonance frequency for different glass thickness and nanomagnetic film stacks. As the glass core thickness reduces from 300 µm to 50 µm, both inductance and Q factor decrease. With decreasing distance between the copper networks separated by thinner glass, parasitic capacitance is induced. This capacitance and inductance of the coil can cause the coil to become self-resonant at

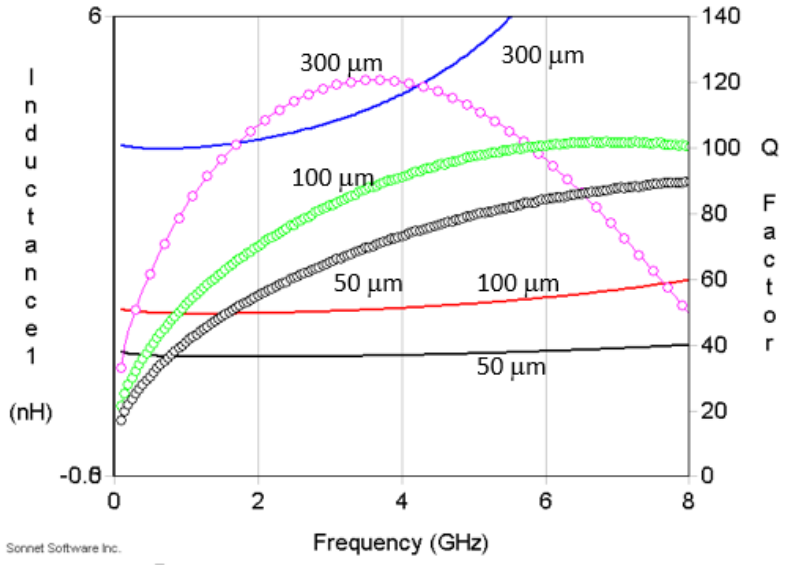
lower frequencies. Excessive parasitic capacitance in the inductor structure can, thus, degrade the Quality factor of the inductor. These results are summarized in Figure 47(a).

By introducing 50nm magneto-dielectrics on either side of the glass core, inductance is increased. With more nanomagnetic film layers in the stack, further enhancement in inductance is seen, as expected. Comparing Case 3 and Case 4, it is clear that, while there is a marginal increase in inductance because of the enhanced flux density, the Q factor degrades dramatically. Nanomagnetic films increase the magnetic flux density and lead to higher inductance. However, their conductivity induces eddy currents in the inductor core, which results in the degradation in Q factor. This is shown in Figure 47(b).

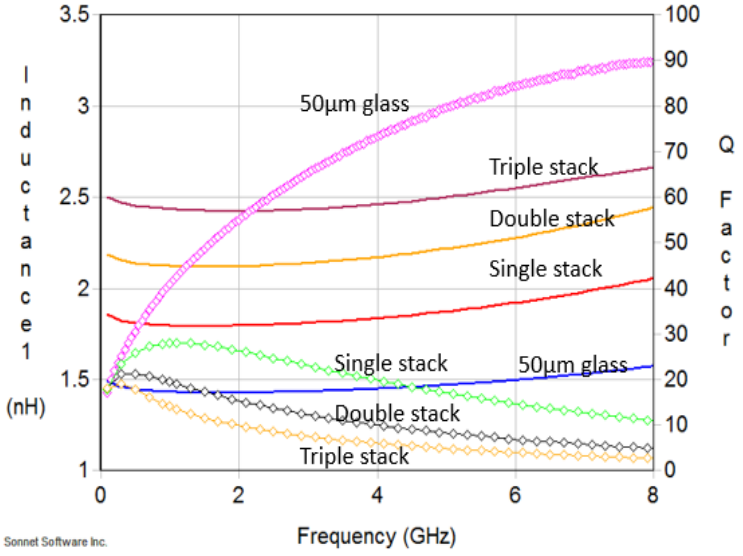
The degradation in Q is addressed with higher-resistivity nanomagnetic films. Parametric analysis with different hypothetical nanomagnetic film resistivities are shown in Figure 47(c). Conductivity of 0.5 Ohm m is required to retain the original Q of the nonmagnetic glass substrates. Such resistivities with high permeability require further optimization in nanomagnetic composition and structure.

Table 15. Simulation result for Inductance, Q factor and SRF.

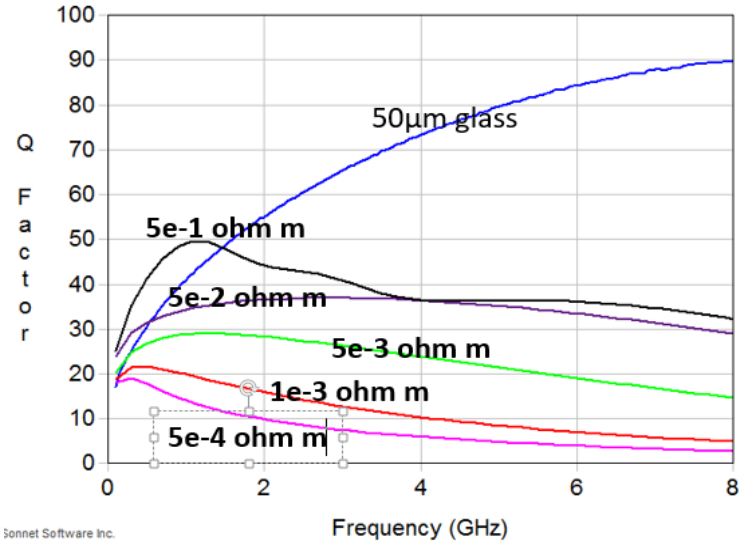
	Inductance at 1GHz (nH)	Q at 1GHz	SRF
Case 1	3.923	82.19	9.65GHz
Case 2	1.946	52.35	>15GHz
Case 3	1.432	40.92	>15GHz
Case 4	1.796	29.03	>15GHz
Case 5	2.121	19.45	>15GHz
Case 6	2.435	14.15	>15GHz


Inductance 1 (nH)
Q Factor
Frequency (GHz)
300 µm
300 µm
100 µm
50 µm
100 µm
50 µm
Sonnet Software Inc.

(a)


Inductance 1 (nH)
Q Factor
Frequency (GHz)
50µm glass
Triple stack
Double stack
Single stack
Single stack
50µm glass
Double stack
Triple stack
Sonnet Software Inc.

(b)



(c)

Figure 47. Simulation results for solenoid inductors: inductance as solid lines, and Q factor as circles. (a): Effect of glass substrate thickness, (b): Effect of nanomagnetic films, (c): Effect of nanomagnetic film resistivity.

Spiral inductors

These 2D inductors are embedded in the top layers above the glass surface. Therefore, glass thickness is not a critical factor for achieving high performance. Single-turn RF inductors wrapped in nanomagnetic films and oxides were designed on a low-loss glass substrate of 100 μm thickness. Figure 48 show a schematic cross-section of the single-turn RF inductor with 3 layers of nanomagnetic films and oxides on either sides of the copper turn. ANSYS HFSS, a 3D EM simulator, was used to simulate the inductors. The ANSYS model for the single-turn RF inductor with wrapped nanomagnetic films and oxides is shown in Figure 48. The X-Y dimensions are 500 μm x 110 μm and copper thickness is 10 μm. Figure 49 also shows the properties of the nanomagnetic film and oxide used in the multilayered structures. In order to study the performance improvements of RF inductors with nanomagnetic films, five cases with different stack of films on the top side are considered, as illustrated in Figure 50.

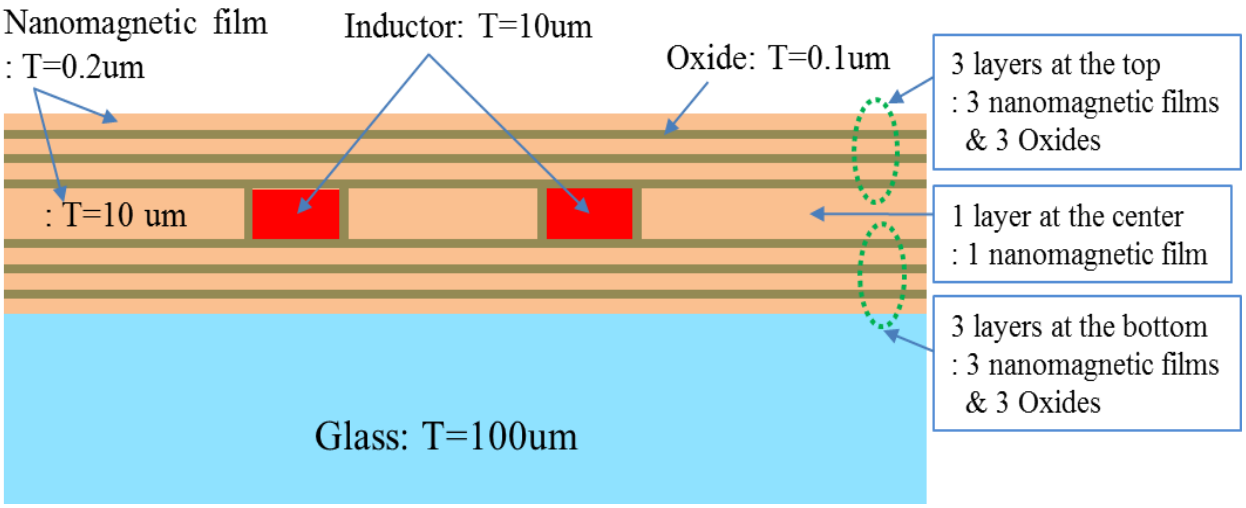


Figure 48. Cross-section of the single-layer RF inductor wrapped around with nanomagnetic films and oxides (um: micron).

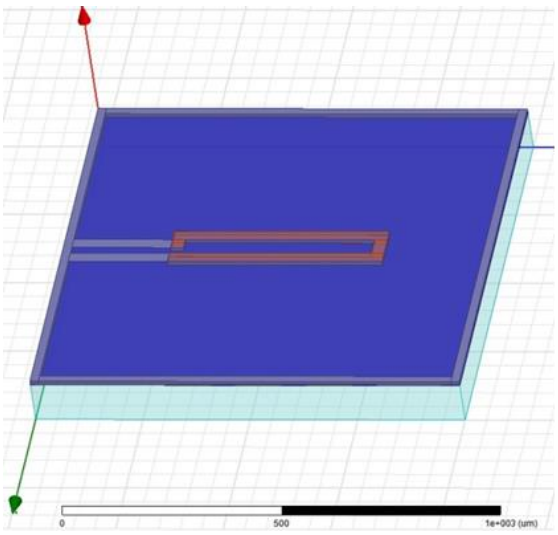


Figure 49. Schematic of the single-layer RF inductor with wrapped nanomagnetic films.

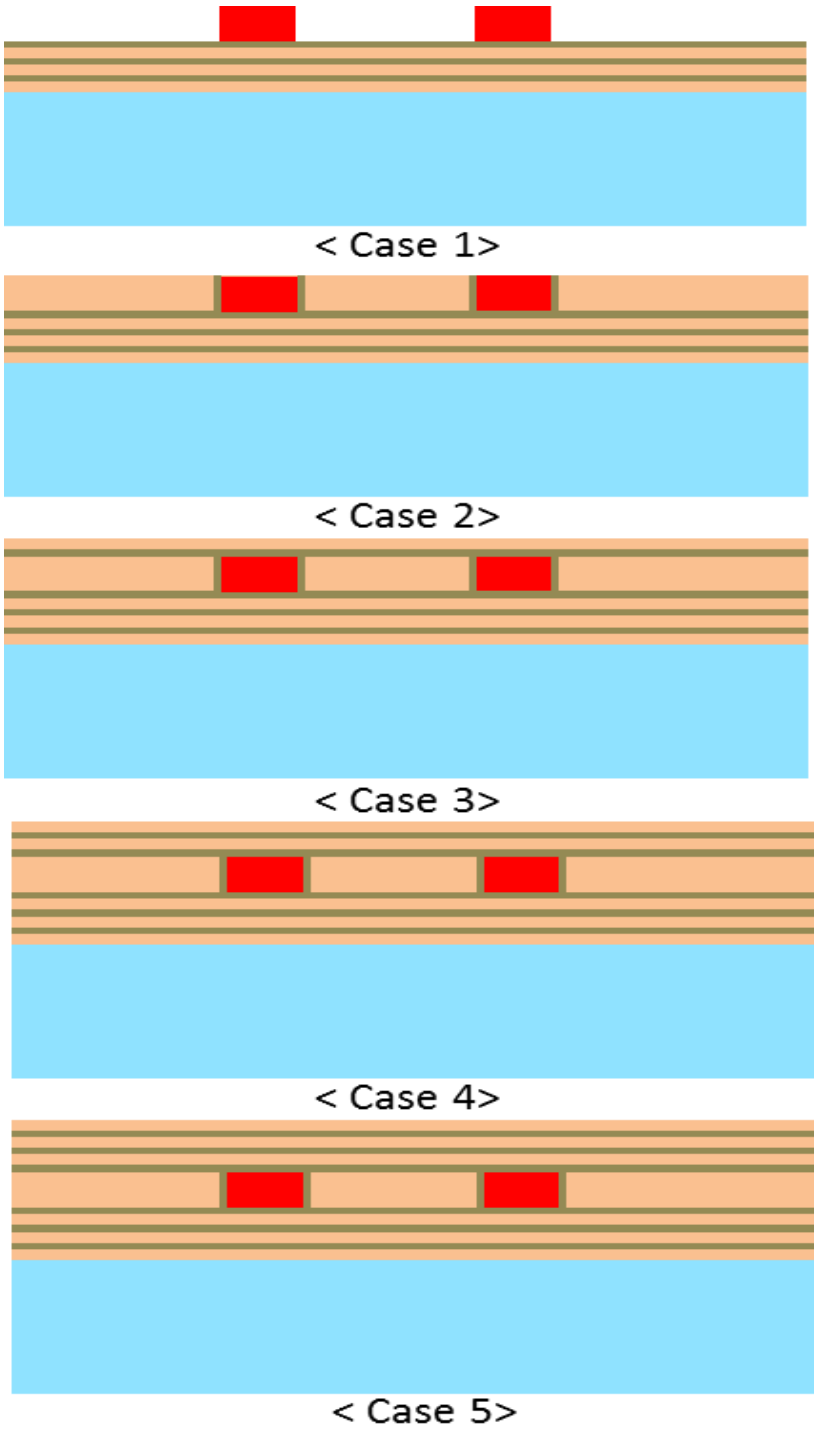
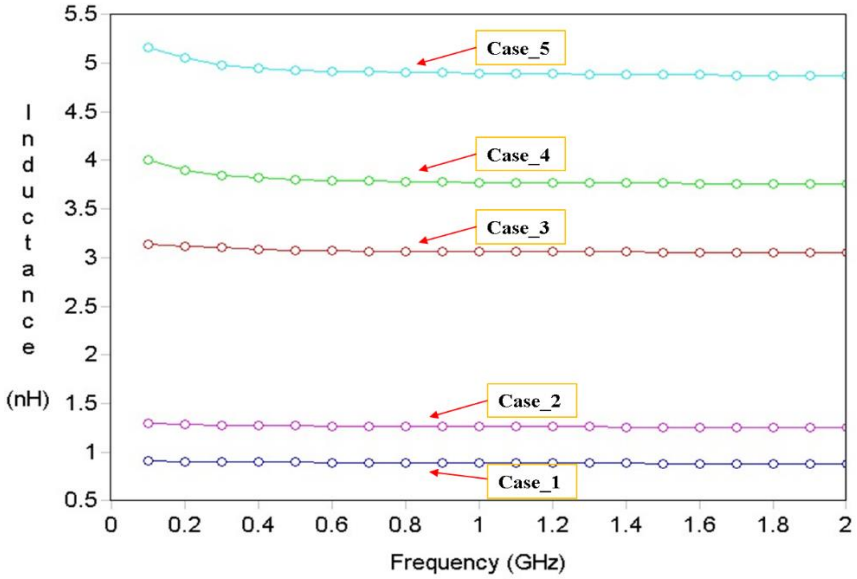


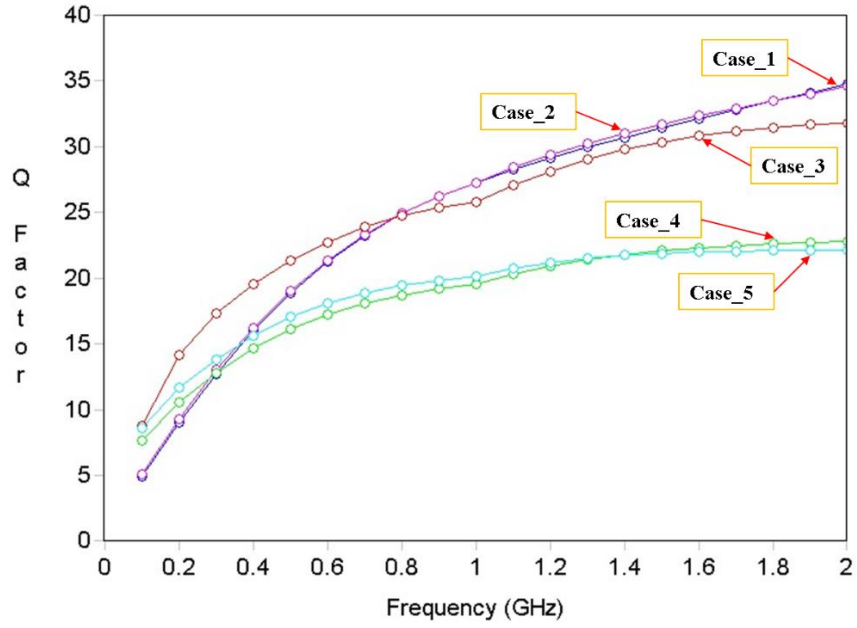
Figure 50. Examples of stack-up for 3D EM simulation of inductors wrapped with nanomagnetic films.

Simulation Results and Analysis

Simulation results for inductance and quality factor versus frequency of the single-layer inductor with five cases of oxides and nanomagnetic film stacks are shown in Figure 51. A notable improvement in frequency response (100 MHz to 2 GHz) of inductance was observed in all the cases with nanomagnetic films. With multiple layers on the top and bottom, an increase in inductance by 5X was achieved, with only 30% degradation in Q at 1.5GHz, these results are summarized in Table 16. Further improvement in Q requires suppression of eddy currents with high-resistivity nanomagnetic films or by introduction of slots in the nanomagnetic films, which requires additional lithography steps for patterning the films. This concept has been demonstrated by Wu et al. [79] The slots truncate the current path to suppress the eddy currents. They also enhance the FMR with their additional shape anisotropy. However, the shape anisotropy degrades the permeability and also increases the hysteresis losses. In spite of this, up to 4.2X increase in inductance and 5X increase in Q compared to nonmagnetic inductors has been achieved. Compared to solenoid inductors, spiral designs with wrapped nanomagnetic films around them showed better inductance without sacrificing Q.



(a)



(b)

Figure 51. Simulation results of (a) inductance and (b) quality factor of inductors wrapped in nanomagnetic films.

Table 16. Summary of 3D EM simulations of inductors wrapped in nanomagnetic films and oxides.

Type	Material thickness	Stack definition	Quality factor	Inductance (nH at 1.5 GHz)
Case 1	Oxide: 0.1 microns Magnetic film: 0.2 microns	3 Bottom layers	31.4	0.89
Case 2		1 Center layer 3 Bottom layers	31.7	1.3
Case 3		1 Top layer 1 Center layer 3 Bottom layers	30.4	3.1
Case 4		2 Top layers 1 Center layer 3 Bottom layers	22.1	3.7
Case 5		3 Top layers 1 Center layer 3 Bottom layers	21.9	4.9

Conclusions

Glass substrate-integrated 2D spiral inductors and through-via-based 3D daisy-chain and solenoid inductors were modeled, designed, fabricated and characterized to quantify their inductance densities, Q factor and SRF, and to assess their suitability for various RF applications. Glass substrate core presents several benefits such as low loss, dimensional stability and low surface roughness for precision circuitry, and moisture- or temperature-insensitive properties for RF applications. Standard low-cost and scalable panel processes are utilized for glass substrate fabrication to make it compatible with high-volume manufacturing (HVM) line. These include high-throughput TPV formation, dryfilm photolithography, precision semi-additive conformal copper electroplating.

Spiral 2D inductors are optimized for high inductance density of 10-20 nH/mm^2, with Q factors of 30-40 at the frequency of the interest. With 3D approaches, better Q of ~70 is achieved by utilizing the Z direction with TPVs for better flux coupling. However, the 3D topologies require 300μm glass to create adequate inductance densities of 3 nH/mm^2. These inductors are applied to matching networks, filters and diplexers for fully-integrated RF modules.

The high-permeability of nanomagnetic films, coupled with high frequency stability and low loss provides new opportunities for inductor miniaturization and performance enhancement in RF sub-systems. For example, nanomagnetic films are suitable for miniaturizing EMI isolation structures either by creating a stack of nonmagnetic and magnetic films, or through microwave absorption from FMR. Nano

magnetodielectrics can also miniaturize and enhance antenna performance by enhancing both permittivity and permeability, while managing the ratio to retain high bandwidth.

Solenoid and spiral inductors were modeled to quantitatively analyze the benefits of nanomagnetic films. With solenoid inductors from nanomagnetic films on glass substrates, 2.5X enhancement in inductance is observed, however, with a dramatic reduction in Q, unless the film deposition process is sufficiently advanced to achieve high resistivity of 0.5 ohm-m. With spiral inductors having nanomagnetic films wrapped above, below and adjacent to the spirals, 5X enhancement in inductance is observed without much degradation in Q. In order to be completely benefit from the nanomagnetic films, along with the eddy current losses from their high conductivity, the losses from high damping factor need to be addressed with suitable chemical and structural modifications. Furthermore, the frequency stability need to be enhanced to above 1.5 GHz with higher field anisotropy and saturation magnetization.

CHAPTER 4

Thermal Management with COPPER TPVs

This chapter addresses the thermal dissipation of power amplifier (PA) chips, which is one of the biggest challenges in the development of ultra-miniaturized glass-based RF modules. Glass packages with 3D or double-side active and passive integration offer the best miniaturization and performance enhancement for RF modules because glass has ultra-low loss, dimensional stability for precision thinfilm components, ability to process through-vias in large panels to reduce cost [80]. However, glass is a poor thermal conductor. Cooling of the high-power PA die with integrated miniaturized RF modules is, therefore, a key challenge. This paper provides extensive modeling studies of RF power amplifier modules with copper thermal vias in ultra-miniaturized glass, without additional process steps. It considers various power amplifier design options such as: a) Si vs. Silicon-on-Insulator (SOI), b) location of die hotspot, c) via geometry, and d) conformal vs. fully-filled vias, and provides optimal design recommendations with modeling and analysis.

The specific objectives of this task are to model, design, fabricate and characterize highly-efficient Cu TPV-based passive thermal structures for cooling the PA die in glass packages. The specific targets are described in Table 17.

Table 17. Specifications for PA cooling.

Specifications	
Power	1W (30 dBm)
Power Efficiency(PAE)	30%
Die Size	3.5mm X 2.5mm
Hot-spot size	350μm X 250μm (10% of die size)
Junction Temp.	185°C
Target Steady-state Temp.	85°C

Geometry of TPVs and their optimal placement in the substrate are critical to transfer heat from the PA hot-spot to the Cu heat-spreader in PCB. Based on the parametric simulations with Cu TPV networks, approximate volume and distribution of copper that can efficiently enhance the heat transfer through the low-conductivity glass substrate is obtained.

Approach

PA thermal dissipation challenge with ultra-miniaturized glass packages is addressed without the need for additional passive and active cooling structures and processes. This is accomplished with low-cost copper through-vias to effectively dissipate the heat from the PA hotspot, as illustrated in Figure 52. Georgia Tech and its partners have shown that glass interposers and packages can be fabricated with ultra-

high-density copper TPVs with low-cost processes [81]. The Cu TPV-based cooling was previously applied to glass interposers by Cho et al. [82]. This paper applies this concept to RF PA modules. The key performance parameters and targets for the modules are shown in Table 18.

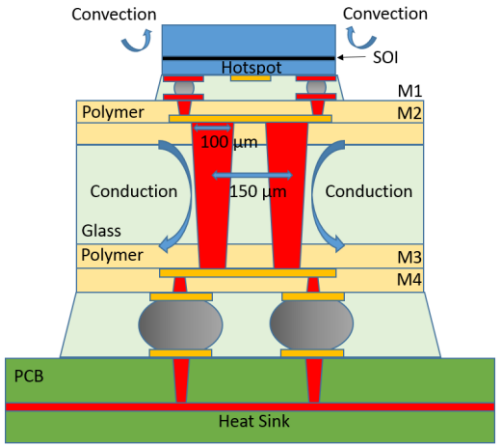


Figure 52. RF PA Module with thermal via structures for effective heat dissipation.

Table 18. PA module parameters and targets

Power	1W
Power Efficiency of PA	30%
PA Die Size	3.5mm x 2.5mm
Hot Spot Size (10% of Die Size)	350µm x 250µm
Junction Temperature	185°C
Target Die Steady State Temperature	85°C

Modeling

A detailed thermal model for cooling PA chips with different thermal via designs was setup using the commercial package COMSOL. The model simulates heat transfer from the PA die that is flip-chip assembled with solder or copper bumps with blind vias

on the build-up layers, with glass TPVs, and then onto the PCB. Different boundary conditions for hotspots where considered. These involve: a) PA with cooling from both top and bottom sides through convection, b) silicon-on-insulator (SOI) with an oxide thickness of 1µm between the active device layer and the silicon, which allows heat transfer predominantly from the bottom side using thermal vias, and c) different hot-spot locations on PA (die edge or die center). Structural variations of thermal vias such as conformal vias vs fully-filled copper vias with various inside and outside via diameters, as well as copper thickness and pitch were also considered.

The structure is composed of multiple layers comprising of PA die, underfill, BGA, blind via, stack-up (polymer-glass-polymer), solder ball, copper pillar, PCB and a heatsink as shown in Figure 53. The top most structure is a PA die: 3.5 mm x 2.5mm in dimensions and 0.1mm in thickness, which could be either CMOS or GaAs. Depending on the simulation scenario, an SOI is also considered above the hot-spot area with 1µm oxide thickness. The hot-spot is located on the bottom surface of PA die. A dissipation power of 0.7 W is imposed on the area, assuming a power efficiency of 30% for a 1 W chip. Six thermal micro-bumps and copper-filled blind vias are considered underneath the hotspot. The blind vias connect the copper pads between M1 and M2. In the stack-up, polymer dielectric is laminated on the top and bottom of the glass surfaces in order to buffer up the physical stress. TPV connects M2 to M3. Copper pillar connects the solder balls to the heat sink in PCB.

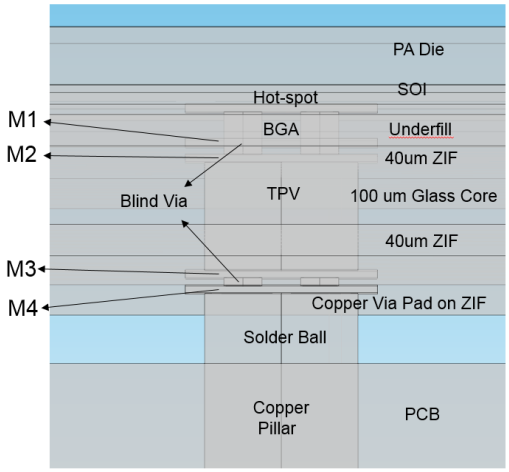


Figure 53. Detailed structure for the modeling setup with COMSOL.

The following boundary conditions were applied for all the simulations.

- Heat Transfer Coefficient: $\underline{H = 10\ W/m^2K}$
- P_{Total} = 0.7 W was imposed on the Hot-spot;
- Heat flux = $\underline{0.7W / (0.25\ mm \times 0.35\ mm) = 8W/mm^2}$

Figure 54 shows one example (six Blind Vias and a TPV) of the model with overall view, side view, and inner view of the structure. The diameter of blind via is 50µm, whereas the pitch is 100µm. A single TPV has a diameter of 200µm. The geometry of the blind via and TPV was tailored for each simulation in order to study the effect of via geometry. Table 19 lists the materials and properties that were used in the COMSOL model construction.

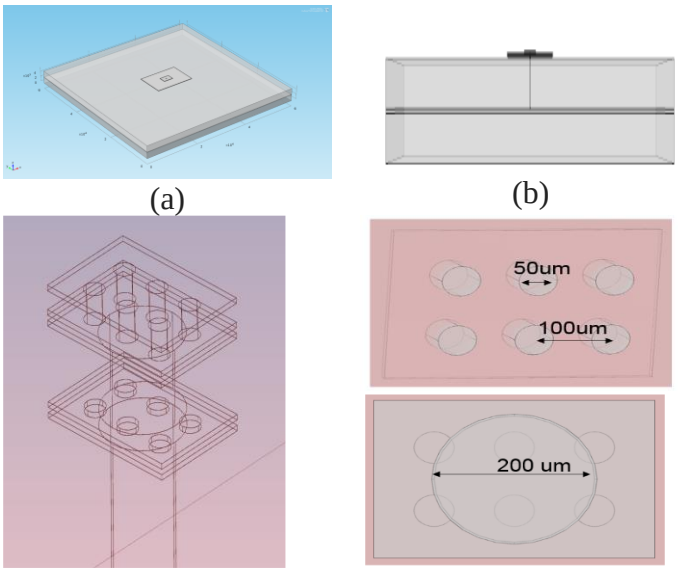


Figure 54**.** COMSOL model construction: (a) Overall View, (b) Side View, (c) Inner View, (d) Diameter and pitch for Blind Via, and TPV.

Table 19. Materials and properties used for the simulation

	Heat Capacity [J/(kg·K)]	Density [kg/m^3]	Thermal Conductivity [W/(m·K)]
FR4	1369	1900	0.3
Silicon	700	2329	130
SOI	1000	2200	1.4
Underfill	800	1510	0.3
Polymer(ZIF)	936	2100	1
Glass	480	2200	1.1
Heat Sink	385	8700	400
Metal Pad	385	8700	400
Blind Via	385	8700	400
TPV	385	8700	400

Simulation Results

Four types of scenarios were modeled: 1) Si vs. SOI, 2) location of die hotspot, 3) via geometry, and 4) conformal vs. fully-filled vias.

Si vs. SOI

With SOI wafers, transistors are formed in the thin layers of silicon that are isolated from the main body of the wafer by a layer of electrical insulator, usually silicon dioxide. Parameter 1 examines if SOI ICs affect the steady-state temperature on the hotspot area. Both the SOI and Si PA have the same number of Cu blind vias and a TPV, with hotspot location either at the center or at the corner. From Table 20, the SOI above the hot-spot blocked thermal conduction through the remaining PA die, resulting in a slight increase in the steady-state temperature.

Table 20. Simulation results for SOI vs. Si

	Model 1	Model 2	Model 3	Model 4
Hotspot Location	Center	Center	Corner	Corner
SOI	No	Yes	No	Yes
Steady-State Temperature	65.4°C	70.2°C	66.5°C	73.6°C

Location of Die Hotspot

Parameter 2 compares the thermal dissipation characteristics when hotspot is located at the center to that at the corner. Comparing Model 1 and Model 3 in Table 21, an insignificant difference in the steady-state temperature was observed, although the die was slightly cooler when the hotspot was at the center (Model 1). An example of simulation result with hotspot at the die corner is shown in Figure 55.

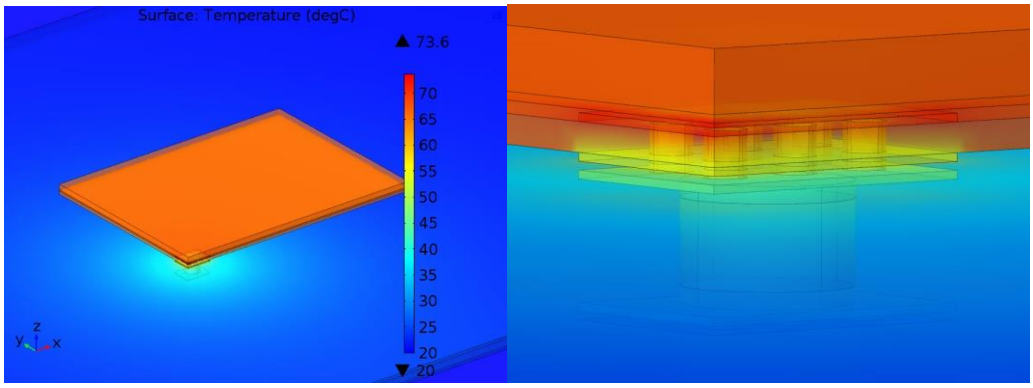


Figure 55**.** An example of simulation result with hotspot at the die corner using an SOI PA die.

Via Geometry

Parameter 3 compares the steady-state temperature with the variations in via geometry. All simulations were conducted with fully-filled copper vias. The numbers of blind vias and TPVs were varied to investigate the cooling effect for each case. Model 1 in Table 22 shows that the most efficient way to cool the PA die is by using a direct TPV connection onto the die without any blind vias. Comparing Model 2 with Model 3, more blind vias with the same number of TPVs improved the heat dissipation from the hotspot. With the same number of blind vias, more TPV copper volume had better heat dissipation. When the total volumetric metallization between blind vias and TPVs is kept constant, the system achieved similar matched steady-state temperatures as seen in Table 21.

Table 21. Simulation results with different via geometries

	Model 1	Model 2	Model 3	Model 4	Model 5	Model 6
B.V. between M1 and M2	0	6	4	6	4	6
B.V. between M3 and M4	0	6	4	6	4	6
No. of TPV	1	1	1	2	2	4
Diameter/ Pitch (Blind Via)	NA	50µm/ 100µm	50µm/ 200µm	50µm/ 100µm	50µm/ 200µm	50µm/ 100µm
Diameter/ Pitch (TPV)	200µm/NA	200µm/NA	200µm/NA	100µm/ 150µm	100µm/ 150µm	100µm/ 150µm
Steady-state Temperature	52.9°C	65.4°C	86.1°C	76.7°C	90.1°C	65.9°C

Conformal vs. Fully-filled Vias

Parameter 4 inspects the impact of via type (conformal vs. fully-filled) and its thermal dissipation performance with variations in metal thickness. For the blind via BV, a diameter of 50µm is used, whereas 200µm is used for TPV's. Table 22 shows the trend of the steady-state temperature depending on the inside metallization thickness of via. The last row of the table illustrates that Model 1 shows the worst case of cooling scenario when both blind via and TPV have conformal metallization with 5µm metal thickness. In contrast, Model 5 demonstrates that when both blind and through vias are fully-filled, they could dissipate the heat most effectively. As the inside copper thickness increases, the steady-state temperature decreases accordingly, as seen from the transition between Model 1 and Model 5.

Table 22. Simulation results with different blind via and TPV combinations

	Model 1	Model 2	Model 3	Model 4	Model 5
Type of B.V.	Conformal	Fully-filled	Fully-filled	Fully-filled	Fully-filled
Type of TPV	Conformal	Conformal	Conformal	Conformal	Fully-filled
Inside Metallization Thickness (Blind via/ TPV)	(5µm/5µm)	(NA/5µm)	(NA/10µm)	(NA/15µm)	(NA)
Steady-state temperature	224°C	129°C	98.4°C	86.9°C	65.4°C

A proper combination of blind via and TPVs can be a very effective design feature for reducing the thermal resistance for multi-layer substrates, especially for glass packages. Thus, it is critical to choose the right via design, appropriate via count and efficient amount of copper metallization to optimize the package thermal design, while meeting the electrical constraints**.** The most efficient method to cool the PA die is to have

a direct interconnection of TPV from the die to heatsink, which results in a steady-state temperature of 52.9°C. In such case, the fully-filled TPV with 200µm diameter would have substantial amount of copper inside, which requires new and innovative approaches for TPV filling. Even with a SOI PA and corner (unfavorable) hotspot locations, various combinations of blind vias and TPVs were able to achieve similar steady-state temperatures of 65.4°C and 65.9°C. Both of them satisfy the target steady-state temperatures of less than 85°C. A combination of via types, having 6 fully-filled blind vias and a single conformal TPV with 15µm thickness of metallization, resulted in a steady state temperature of 86.9°C, only slightly more than the target temperature at 85°C. Thus, further increase in the inside metallization (>15µm) would be able to meet the target steady-state temperature requirements at relatively low-cost because conformal vias take less time to electroplate.

Conclusions

Ultra-thin glass-based power amplifier modules with copper through-vias were modeled for its thermal conduction characteristics. The impact of various design parameters was investigated through modeling to determine their efficacy in thermal management of power amplifier ICs. The location of hotspot was modeled as the first design parameter. The steady-state temperature did not vary significantly when the hotspot is either at the center or at the edge. The small difference comes from the availability of more easily accessible surface area for heat spreading when the hotspot is at the die center. The second parametric study compared Si with SOI. In SOI, the oxide that isolates the Si from the device layer blocks the heat-transfer from the hotspot to the

remaining part of PA die because of its poor thermal conductivity, resulting in a slight increase of the steady-state temperature. The models also quantitatively confirmed that the most efficient way to cool the PA die was to have a direct TPV with no blind vias since it provides the lowest thermal impedance. The steady-state temperature was lower with increasing number of blind vias or volumetric copper metallization. As the copper metallization inside the conformal via gets thicker, the steady-state temperature correspondingly decreases. The fully-filled copper vias provided the best option for PA cooling.

Extensive thermal parametric simulations were performed to verify the thermal performance of Cu TPV networks embedded in glass substrates. Based on the simulation results, diameter, pitch, number and location of thermal vias were designed to efficiently transfer the heat from the die to the copper heat-spreader in PCB.

CHAPTER 5

Dual-band WLAN Glass Modules

Advanced RF packages with active (low-noise amplifier, RF switch) and passive integration in ultra-thin 3D glass packages are demonstrated with miniaturization and enhanced performance. The novelty of this RF packages is three-fold: 1) Ultra-thin 100 μm glass, 2) Double-side thinfilm RF circuits interconnected with Through-Package Vias (TPVs), and 3) Direct assembly of the glass-core package to the board with Land Grid Array (LGA) connections. An innovative double-via process, starting from prefabricated vias in bare glass, polymer filling and via drilling, is utilized for a robust and high-yield substrate fabrication process. Scalable and low-cost panel laminate processes are utilized to form the RF circuits on the build-up layers. The performance benefits are demonstrated through interconnect loss, impedance match, electrical gain and noise figure measurements. Compared to existing RF substrates, the glass substrates show 2.5X miniaturization in substrate thickness with extensibility to thinner substrates.

Objective

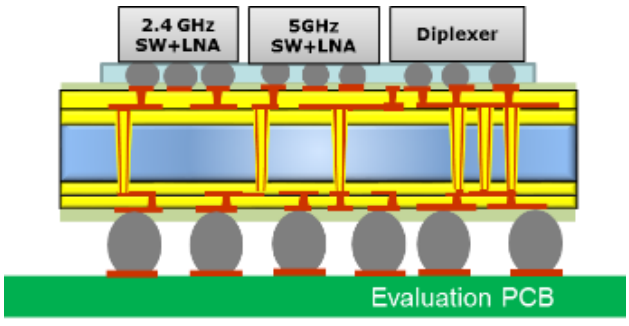
The objectives of this task are to design, fabricate, characterize and demonstrate ultra-thin glass substrates for WLAN modules with enhanced electrical performance. The objectives are summarized in Table 23.

Table 23. Objectives for glass substrate

Parameters	Metrics	State-of-the-art	targets
Fabrication	Loss from entrance to exit port	1-2 dB	0.5 -1 dB
	Substrate Thickness	300 µm	3X reduction: 100 µm
	TPV diameter	200 µm	100 µm
	Lines/spaces	50 µm	15 µm

Package Test-vehicle layout

Details of the RF package design is beyond the scope of this paper. A brief overview of the RF package layout is discussed here. The block diagram of WLAN system is depicted in Figure 56. The dotted red rectangle in the diagram elaborates the schematic of Rx system. It contains 2.4GHz/5GHz LNAs, RF Switch and diplexer. The fabricated Rx module with glass substrate consists of four metal layers with fine-line RDLs and Through-package-vias (TPV), and it interconnects the active and passive components, and the PCB.



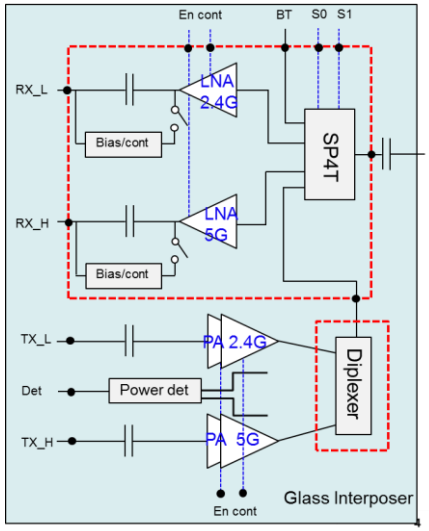


Figure 56. (a) Rx part of WLAN Module

(b) Block diagram of WLAN Module

The transmitter (Tx) and receiver (Rx) parts of a dual-band WLAN front-end-module (FEM) comprises of LNA, PA and switch as the primary active components, and passive components such as diplexer, matching networks, and decoupling capacitors. Floor planning optimization should be preceded prior to design to minimize interconnection length between chip and various devices.

After effective placement of chips and devices is completed through floor planning, signal analysis is performed to design the most optimal interconnection between the actives. To minimize the loss of signal at the target frequency of dual band WLAN, two aspects should be considered: signal matching and stable return current path. Since there is a significant difference between the physical dimensions of pads and signal

lines (RDL) for each chip and devices, it is very important to determine the optimal design rules based on such design constraints. Process ground rules are shown in Figure 57. In addition, since the signal transmission characteristics can be degraded due to the crosstalk between signal lines, it is important to design for impedance matching and crosstalk attenuation, and it is also essential to select appropriate signal line type accordingly.

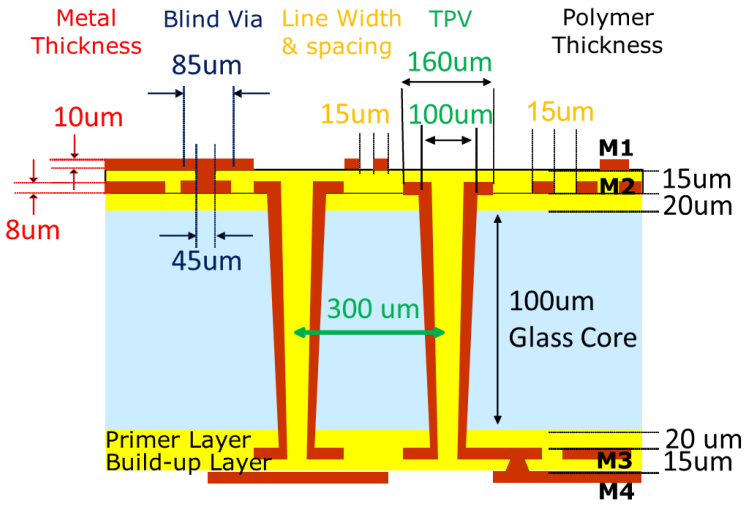


Figure 57. Process ground rules for 3D WLAN Module

It is also important to support a stable reference for the module by placing a ground at the proper place to carry the signal. By designing the ground plane on both sides of the glass substrate, stable references can be made to all the pins and signals, thus benefiting from the 3D IPAC architecture. By thus ensuring proper return current paths, the return noise between the signal lines can be reduced in order to improve the signal transmission characteristics. Based on this design, it is possible to meet the target total

system gain by optimizing the signal transmission characteristics in the glass interposer. The overall system is constructed such that the noise coupling does not degrade the Noise Figure (NF) value.

Several considerations are also required for the mask layout. Firstly, the empty spaces between copper networks in the coupon should be properly filled with rectangular copper dummy mesh in order to enhance the uniformity in copper thickness throughout the package, and prevent over-etching of the fine-line circuits. The amount of copper on both sides of the glass should be matched to prevent any warpage. Dicing constraints also need to be considered for the panel layout.

Materials and Processes

Materials

The substrate stack-up and process ground rules that are employed in the design and fabrication of the WLAN module substrate are depicted in Table 24 and Figure 57. The substrate core is an alkali-free glass with 100 µm thickness, laminated with a 20µm thick dry film polymer. The build-up layer consists of a dry-film polymer dielectric with a thickness of 15 µm. The diameter of the TPVs in the glass core is 100 µm, and that of the blind vias in the polymer build-up layer is 45 µm. The minimum line width and spacing is 15 µm, with the metal thickness on each layer being 8µm for the inner copper layer (M2 and M3) and 10µm for the outer copper layers (M1 and M4).

Table 24. Materials used for the glass fabrication

Stack-up		
Layer	Thickness (μm)	Material
M1	8μm – 10μm	Cu
Build-up Top	15μm	GX-92 (Ajinomoto; Epoxy dielectric)
M2	8μm	Cu
Primer Top	20μm	GX-92 (Ajinomoto; Epoxy dielectric)
Core	100μm	Corning Glass
Primer Bottom	20μm	GX-92 (Ajinomoto; Epoxy dielectric)
M3	8μm	Cu
Build-up Bottom	15μm	GX-92 (Ajinomoto; Epoxy dielectric)
M4	8μm – 10μm	Cu

Fabrication Process

The process flow for fabricating the glass substrates with TPVs and RDL is shown in Figure 58. Direct formation of TPVs by UV laser ablation of polymer-laminated glass substrates faces challenges because of excess damage near the entrance and exit of the vias. This damage affects the quality of copper metallization around the

TPVs, resulting in low yields of the 3D interconnects. An improved process using pre-fabricated through-vias in bare glass, followed by polymer lamination and second via formation was used. For this process, through-vias are first formed in bare glass panels by the supplier (Corning Inc, New York). The glass panels with prefabricated TPVs are cleaned using organic solvents (acetone, methanol and Isopropyl alcohol) to remove residues and impurities. Following this, thin dry-film polymers (ABF GX-92 from Ajinomoto Co., Inc., Japan) with a thickness of 20 µm are laminated onto both sides of the glass substrate. The polymer flows and completely fills the glass vias. A second laser process is then used to form smaller through-vias inside the polymer filling of the pre-drilled glass vias, creating the double-via structures.

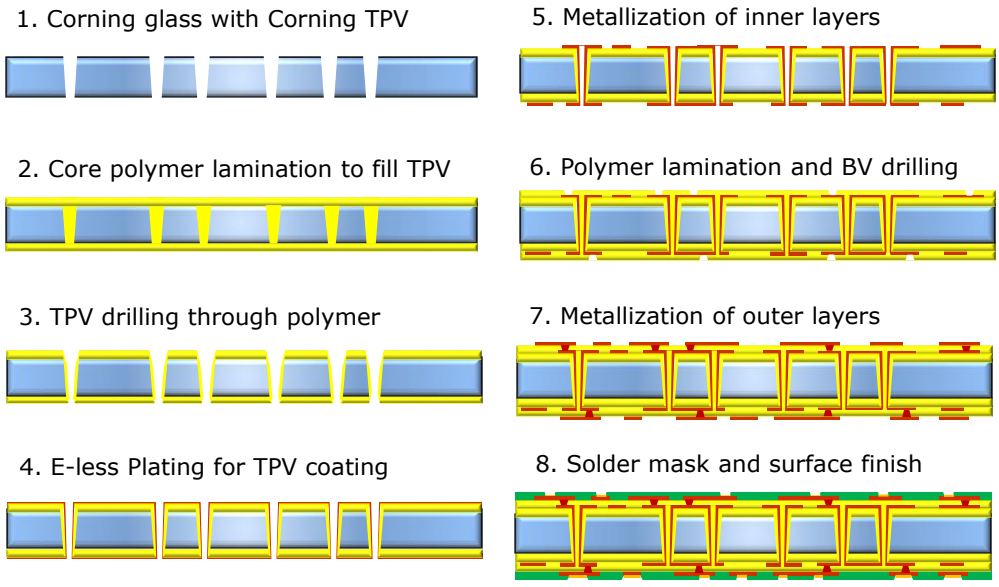


Figure 58. Detailed process flow for 4ML WLAN module fabrication

This process results in a polymer liner on top, bottom and side walls of the TPVs, simplifying via metallization and improving reliability by eliminating direct copper plating on glass surfaces. Figure 59 demonstrates the successful metallization of 70µm diameter through vias in the polymer inside pre-drilled 100µm glass vias in 100µm thick glass substrates. Compared to prevalent 0.5 mm RF substrates, these substrates feature 2.5X lower thickness.

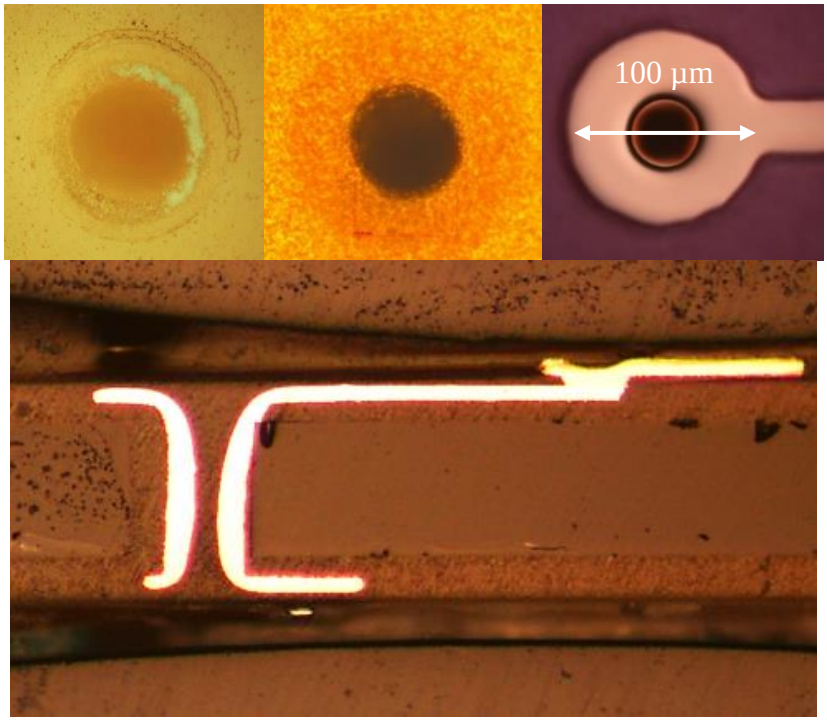


Figure 59. (a) TPV after double-via drilling, electroless plating on TPV, and metallization of TPV, (b) Cross-section of the glass substrate.

Semi-additive plating (SAP) process is used to metallize the TPVs, starting with electroless copper seed layer deposition. Dryfilm photoresist lithography is used to define the circuit patterns on the top and bottom of the glass core, followed by copper electroplating to simultaneously metallize the TPVs and RF circuit patterns on both sides. The targeted copper thickness for inner metal layers (M2 and M3) is 8 µm.

In order to complete the four-metal-layer fabrication, the process is continued with the lamination of additional polymer dry films on both sides of the two–metal-layer substrates. UV laser-ablated micro-vias are formed in the build-up polymers to interconnect them to the core metal layers. Semi-additive patterning approach is used to metallize and pattern the surface metal layers. This step is followed by solder-mask patterning to selectively passivate the surfaces. Electroless nickel immersion gold (ENIG) surface finish is plated onto the chip-bonding pads. A completed four-metal layer glass substrate with TPVs and double-side RF circuit layers is shown in Figure 60.

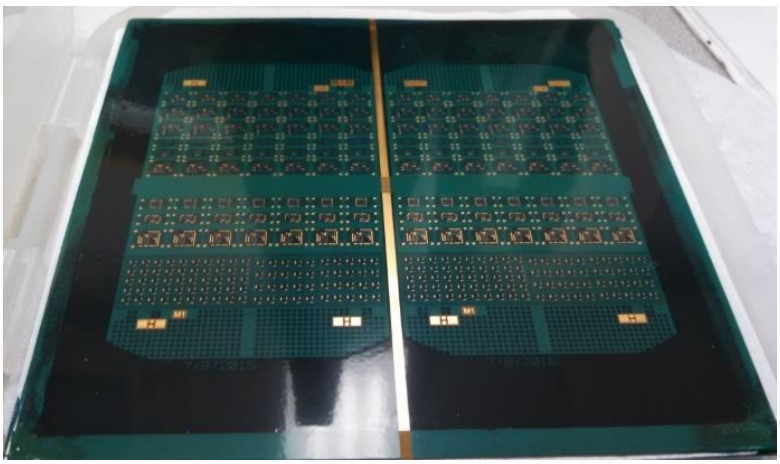


Figure 60. Fabricated Samples of 3D WLAN module

Module Assembly

LNA and switch assembly was performed with a standard lead-free solder reflow process. As a first step in the assembly process, NR200 flux was applied to the bond pads. Component placement was performed with a Finetech MatrixTM flip-chip bonder. Assembly was performed with a reflow profile customized for glass substrates. The peak temperature was 260°C and the dwell time at the reflow temperature was 2 minutes. The assemblies were then underfilled with a commercial underfill (ME-531 from Lord Corporation) by capillary flow. The substrates were preheated to 100°C for the underfill flow. This is followed by underfill curing at 150°C for 30 min. Optical micrographs of the fabricated substrate and assembled test-vehicle are shown in Figure 61. The glass packages were assembled onto boards with LGAs. The approximate pad size is 300 microns and the pad opening is 200-220 microns. The PCB pitch is 500 µm. An image of the module assembled on the board is shown in Figure 62.

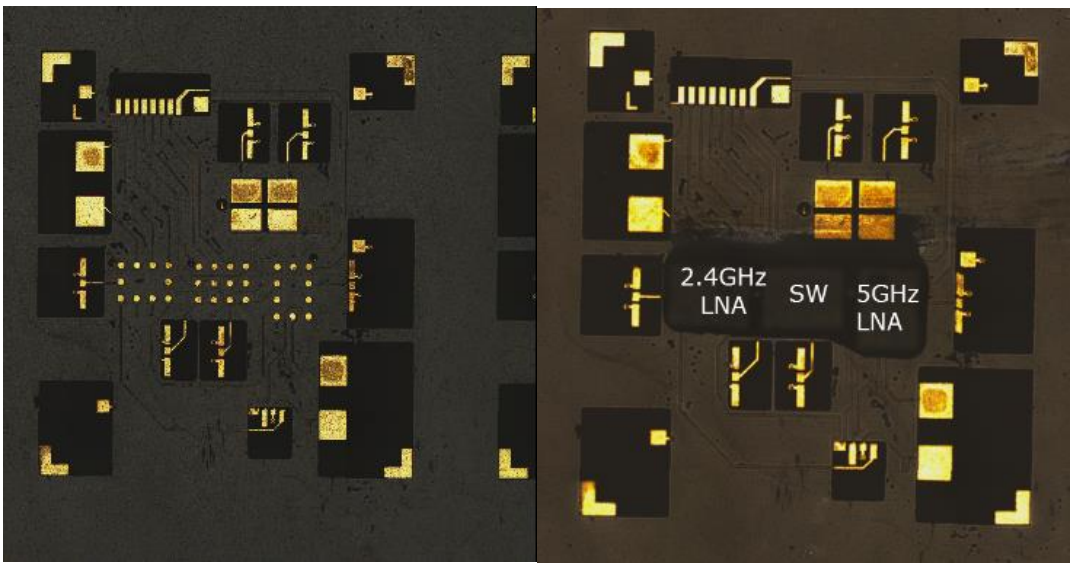


Figure 61. (a) WLAN module before die-assembly;

(b) WLAN module with assembled dies.

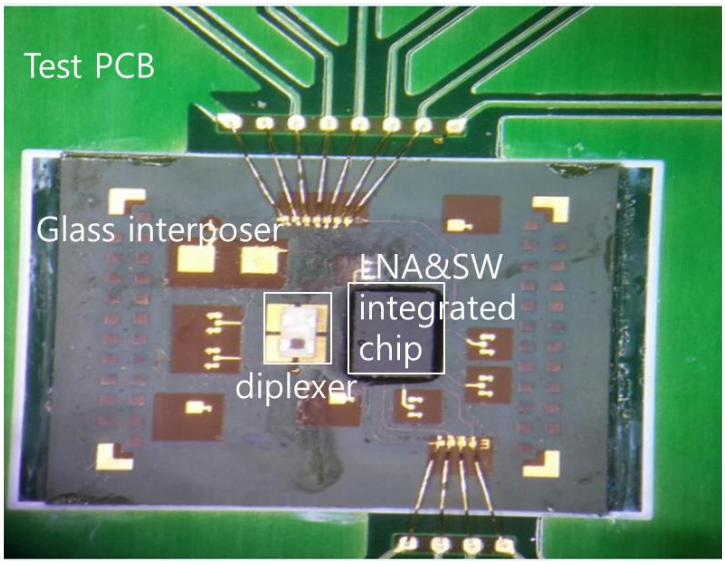


Figure 62. Assembled WLAN module

Electrical characterization of 3D glass module for WLAN

In order to demonstrate the module integration in glass packages, three classes of electrical characterization are performed: a) Impedance along different RF paths, b) Trace insertion loss between actives and passives, c) Module characterization through gain and noise figure measurements. These results are described below.

a) Impedance along different RF paths:

The characteristic impedances of the fabricated traces should match well with the target of 50Ω. If the conductor is of a uniform 50Ω impedance and is properly terminated, there will be no reflections and the incident signal will be absorbed at the far-end by the

termination. Instead, if there are impedance variations, some of the incident signal will be reflected to the source. The characterized traces are indicated with red box and numbered as illustrated in Figure 67(a). The simulation results for the characteristic impedances of RF paths show 50.1-50.3Ω, as compiled in Table 25. For each current path, impedances were measured in order to correlate them with the simulation data. All the measured data are within the acceptable ranges, having extra 2Ω to 3Ω in comparison to the simulated value of 50Ω. However, given the fact that there are ohmic contact losses while landing the probes on the pads, the measured impedances are still in good correlation with the simulation, thus, minimizing the signal loss between the two ports. This confirms minimal signal reflections from the impedance mismatch.

Table 25. Simulation and measurement correlations for the characteristic impedance in different RF paths

	RF paths			
	5 GHz switch to LNA	2.4 GHz switch to LNA	Diplexer to 5 GHz switch	Diplexer to 2.4 GHz switch
Simulation	50.34 Ω	50.25 Ω	50.14 Ω	50.11 Ω
Average Impedance	53.90 Ω	54.35 Ω	53.08 Ω	53.26 Ω
Standard deviation	0.13	0.23	0.22	0.20

b) Trace insertion loss: The insertion loss in traces indicates the energy lost when current flows through the conductor. To examine the quality of fabrication, several critical paths, including switch-to-LNA and switch-to-diplexer were selected and characterized for both low and high bands. In order to study the variation in signal loss, insertion loss for each corresponding path was measured on four individual samples and organized into the best and worst cases. This correlation quantifies the yield in RDLs and vias in package, which is sensitive to open/short defects. In addition, by measuring the insertion loss in selected critical traces, the overall quality of glass fabrication is also validated. Frequency sweep from 100MHz to 10GHz was performed on four critical paths. The results are tabulated in Table 26. An example of measurement from diplexer to 2.4GHz switch is also shown in Figure 63(c). The insertion loss is consistently low for all the cases, and matches well with the full-wave EM solver HFSS simulation. Considering the measurement errors, such as calibration error and contact error, the simulation and the measurement results are in good correlation.

Table 26. Insertion loss measurement and simulation correlation for four critical RF paths in the RX package

	RF paths			
	5 GHz switch to LNA	2.4 GHz switch to LNA	Diplexer to 5 GHz switch	Diplexer to 2.4 GHz switch
Simulation	0.07dB	0.055dB	0.06dB	0.03dB
Best-case measurement	0.09dB	0.06dB	0.013dB	0.04dB
Worst-case measurement	0.19dB	0.19dB	0.015dB	0.06dB

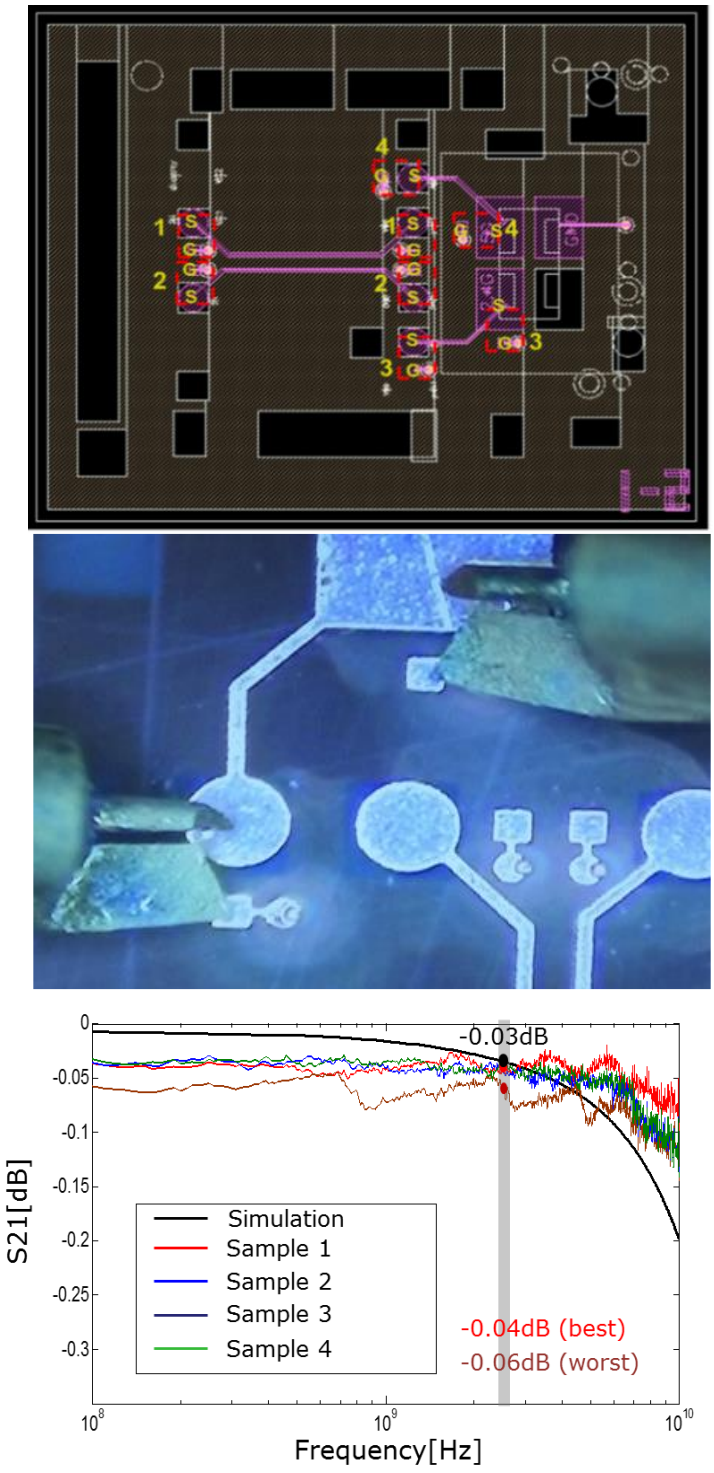


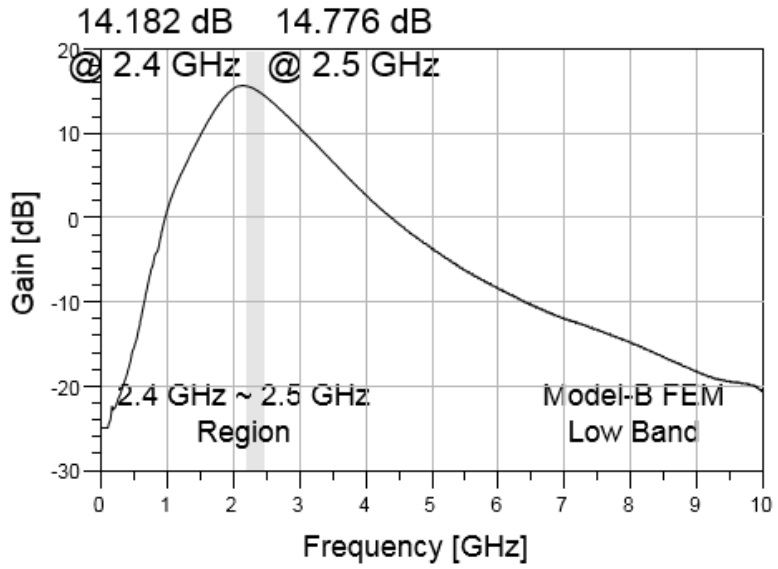
Figure 63. (a) Measured paths for insertion loss and characteristic impedance

(b) Optical micrograph of the measured traces, (c) An example of measurements from Diplexer to 2.4GHz Switch

c) Module Characterization: Electrical performance characterization of active components was performed with high-precision RF GSG probes. Rx gain and noise figure for two separate bands – 2.4GHz and 5GHz – were measured. The targets and the measured data of Rx gain and noise figure for both bands are compiled in Table 27. For low band, the measured value of Rx gain (14.39dB) met the target of 14dB, and the measured noise figure (2.1dB) met the requirement of <2.5dB, as shown in Figure 64. For high band, the measured Rx gain (9.5dB) was less than the targeted value of 12dB. However, it can be enhanced with better circuit matching and design improvements. The measured noise figure for high band (2.8dB) also met the target of <3dB.

Table 27. Test goals and Measurements

	Low Band 2.4GHz – 2.5GHz	**High Band 4.9GHz – 5.85GHz**
Rx Gain	Goal: 14dB Measured: 14.39dB	Goal: 12dB Measured: 9.5dB
Noise Figure	Goal: 2.5dB Measured: 2.1dB	Goal: 3dB Measured: 2.8dB



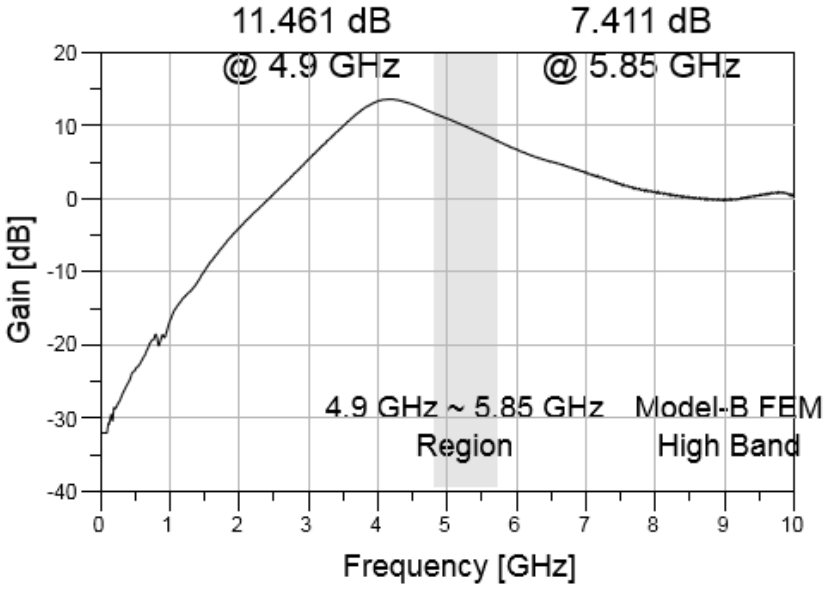


Figure 64. (a) WLAN FEM 2.4GHz Rx gain Measurement

(b) WLAN FEM 5GHz Rx gain Measurement

Conclusions

Glass packages offer several benefits such as precision lithography for impedance matching, low dielectric loss for low insertion loss, high-density wiring for shortest interconnection lengths, and extensibility to 3D component integration with fine-pitch through-package vias, high modulus and CTE match to silicon leading to minimal warpage. This makes glass a compelling substrate alternative for RF module integration.

Glass packages were demonstrated for WLAN receiver module applications with double-side RF circuits, interconnected with TPVs and surface-assembled actives and passives that include LNA and switch. The fabricated modules did not degrade the IC performance metrics such as gain and noise figure, indicating that the package parasitics add minimal insertion losses of less than 0.1dB for critical RF paths. The results also confirm 50 Ω impedance for each RF path from one component to the other, which glass substrates enable with their dimensional stability and precision-lithography. Further, the glass package substrates are 2.5X smaller in thickness compared to LTCC and organic substrates, and are compatible with low cost and scalable panel-processing. This base technology is extensible to integrated Tx + Rx WLAN, LTE and 5G modules in a single glass package with further thickness reduction by utilizing 50 micron glass substrates.

CHAPTER 6

SUMMARY AND FUTURE WORK

Today's RF subsystems are 2D single or multichip packages made of either organic laminates or LTCC (low temperature co-fired ceramic) substrates. The need for form-factor reduction in RF subsystems in both z and x-y direction has led to the evolution of embedded die-package architectures in thin laminates with dies facing up or down. This also reduces insertion loss and improves signal integrity by minimizing package parasitics and routing issues. For further improvement in performance and miniaturization, Georgia Tech proposed and is developing glass as an ideal next-generation substrate for RF module integration. However, major design and fabrication challenges needed to be addressed to achieve ultra-thin high Q RF components and also enable IC cooling to eliminate hotspots on glass substrates. This forms the key focus of this thesis.

Innovative high-Q (>100) and high-density (1-3 nH/mm^2) 3D inductors using through-package via (TPV)-based copper networks in ultra-thin glass substrates were developed and demonstrated in the first part of this research. Copper TPV networks that meet the PA design constraints were designed to enable heat transfer in ultra-miniaturized glass packages and maintain junction temperatures of less than 95^{o}C. Dual-band WLAN RF front-end modules with 3D or double-side thinfilm passive components on glass-based substrates and surface-assembled PA, LNA and switch are fabricated and characterized to demonstrate the benefits of glass-based RF modules.

Ultra-thin High-Q inductors

Glass substrate-integrated 2D spiral inductors and through-via-based 3D daisy-chain and solenoid inductors were modeled, designed, fabricated and characterized to quantify their inductance densities, Q factor and SRF, and to assess their suitability for various RF applications. Glass substrate core presents several benefits such as low loss, dimensional stability and low surface roughness for precision circuitry, and moisture- or temperature-insensitive properties for RF applications. Low-cost and scalable panel processes were utilized for glass substrate fabrication to make it compatible with high-volume manufacturing (HVM) line. These include high-throughput TPV formation, dryfilm photolithography, and precision semi-additive patterning for fabricating the copper RF circuits and interconnects.

Spiral 2D inductors were optimized for high inductance density of 10-20 nH/mm^2, with Q factors of 30-40 at the frequency of the interest. With 3D approaches, better Q of ~70 is achieved by utilizing the Z direction with TPVs for better flux coupling. With advanced designs, Q of 150-200 was achieved with inductance densities of 1.1 nH/mm^2. However, the 3D topologies require 300μm glass to create adequate inductance densities of 3 nH/mm^2. With innovative designs and processes, thinner inductors with 50 microns glass were also designed, fabricated and characterized. Inductance densities of 2.4 nH/mm^2 and Q of 55 were achieved with innovative triangular solenoid designs. These inductors are applied to matching networks, filters and diplexers for fully-integrated RF modules.

The high-permeability of nanomagnetic films, coupled with high frequency stability and low loss provides new opportunities for inductor miniaturization and performance enhancement in RF sub-systems. Solenoid and spiral inductors were modeled to quantitatively analyze the benefits of nanomagnetic films. With solenoid inductors from nanomagnetic films on glass substrates, 2.5X enhancement in inductance is observed, however, with a dramatic reduction in Q, unless the film deposition process is sufficiently advanced to achieve high resistivity of 0.5 ohm-m. With spiral inductors having nanomagnetic films wrapped above, below and adjacent to the spirals, 5X enhancement in inductance is observed without much degradation in Q.

Thermal Management

An ultra-thin glass-based power amplifier module with copper through-vias was modeled for its thermal conduction characteristics. The impact of various design parameters was investigated through modeling to determine their efficacy in thermal management of power amplifier ICs. The location of hotspot was modeled as the first design parameter. The steady-state temperature did not vary significantly when the hotspot is either at the center or at the edge. The small difference comes from the availability of more easily accessible surface area for heat spreading when the hotspot is at the die center. The second parametric study compared Si with SOI. In SOI, the oxide that isolates the Si from the device layer blocks the heat-transfer from the hotspot to the remaining part of PA die because of its poor thermal conductivity, resulting in a slight increase of the steady-state temperature. The models also quantitatively confirmed that

the most efficient way to cool the PA die was to have a direct TPV with no blind vias since it provides the lowest thermal impedance. The steady-state temperature was lower with increasing number of blind vias or volumetric copper metallization. As the copper metallization inside the conformal via gets thicker, the steady-state temperature correspondingly decreases. The fully-filled copper vias provided the best option for power amplifier cooling.

Extensive thermal parametric simulations were performed to verify the thermal performance of Cu TPV networks embedded in glass substrates. Based on the simulation results, diameter, pitch, number and location of thermal vias were designed to efficiently transfer the heat from the die to the copper heat-spreader in PCB.

WLAN module (RF module)

Glass packages offer several benefits such as precision lithography for impedance matching, low dielectric loss for low insertion loss, 3D or doubleside high-density wiring with through-vias for shortest interconnection lengths, extensibility to 3D passive-active component integration with fine-pitch through-package vias, high modulus and CTE match to silicon for enhanced reliability and minimal warpage. This makes glass a compelling substrate alternative for RF module integration.

Glass packages were demonstrated for WLAN receiver module applications with double-side RF circuits, interconnected with TPVs and surface-assembled actives and passives that include LNA and switch. The fabricated modules did not degrade the IC

performance metrics such as RF Gain and noise figure for each band (2.4GHz/ 5GHz), indicating that the package parasitics add minimal insertion losses of less than 0.1dB for critical RF paths. The results also confirm 50 Ω impedance for each RF path from one component to the other, which glass substrates enable with their dimensional stability and precision-lithography. Further, the glass package substrates are 2.5X smaller in thickness compared to LTCC and organic substrates, and are compatible with low cost and scalable panel-processing. This base technology is extensible to integrated Tx + Rx WLAN, LTE and 5G modules in a single glass package with further thickness reduction by utilizing 50 micron glass substrates.

KEY CONTRIBUTIONS

The key contributions from this dissertation are summarized as follows:

- Model, design, fabrication, and characterization of 2D spiral-based inductors and 3D inductors embedded in 3D glass packages with highest Q factor for the target inductance densities and thicknesses

- Characterization of the impact of the fundamental properties of nanomagnetic films on inductor's electrical performance

- Parametric studies of conformal Cu-based thermal vias for heat dissipation from PA hotspot, and validation with thermal measurements of die-package-PCB assembled test vehicle, leading to design guidelines for low junction temperatures in PA modules with ultra-thin glass packages

- First demonstration of Dual-band (2.4GHz/ 5GHz) WLAN module with both Tx and Rx systems in ultra-miniaturized glass packages (100 μm).

FUTURE RESEARCH DIRECTIONS

Ultra-thin High-Q inductors

RF inductors are based on three performance metrics: inductance density, high Q factor and thickness miniaturization. With reduction in inductor thickness, trade-offs between inductance density and Q factor are inevitable. Higher inductance density requires large coil length with current nonmagnetic cores, which invariably degrade the Q factor. Nanomagnetic films can reduce the coil length to achieve the same inductance density and thus increase the Q. In order to be completely benefit from the nanomagnetic films, along with the eddy current losses from their high conductivity, the losses from high damping factor need to be addressed with suitable chemical and structural modifications. Furthermore, the frequency stability need to be enhanced to above 1.5 GHz with higher field anisotropy and saturation magnetization. With these advances, high inductance density can be achieved while still retaining high Q factor for emerging RF applications.

Thermal Management

Thermal test vehicles were modeled and designed, fabricated in order to validate the benefits of thermal management with copper through-vias in glass. Functional test-vehicles with functional RF power amplifier chips with input and output RF paths, substrate-integrated matching networks and copper through-vias need to be demonstrated as the next step. Local heating in the PA and the associated hotspots can degrade the

performance of passives. The interaction between thermal paths and passives need to be considered while designing the modules. Complete module-level design optimization is required while also considering the process design rules that come from the fabrication constraints.

RF Module

RF systems are evolving from the current 4th generation (4G) communications to 5th generation (5G) mobile networks or 5th generation wireless systems. The next-generation telecommunications standards beyond the current 4G standards achieve higher capacity, enabling higher mobile broadband users and supporting device-to-device, ultra-reliable and massive machine communications. Several advances in substrate and module integration are needed to realize 5G systems. These include: lower interconnection losses and precision impedance matching, through-via transitions with lower loss, antenna integration in package for lower system parasitics between the transceiver and the antenna, integration of passive components such as matching networks, decoupling networks and others. Glass fan-out packaging is a compelling technology to address this need for low system parasitics and thinner modules. The glass substrate technologies need to be sufficiently advanced to meet 5G needs. These include achieving better tolerance, fine through-vias and antenna integration with innovative designs.

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